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AFML-TR-75-156

MANUFACTURING TECHNOLOGY FOR RADIATION-HARDENED MULTIPLE IC CHIP PACKAGE

FAIRCHILD CAMERA AND INSTRUMENT CORPORATION
FAIRCHILD SEMICONDUCTOR
MOUNTAIN VIEW, CALIFORNIA

September 1975

TECHNICAL REPORT AFML-TR-75-156

Final Report for Period May 1974 - May 1975

AIR FORCE MATERIALS LABORATORY
Air Force Wright Aeronautical Laboratories
Air Force Systems Command
Wright-Patterson Air Force Base, Ohio 45433

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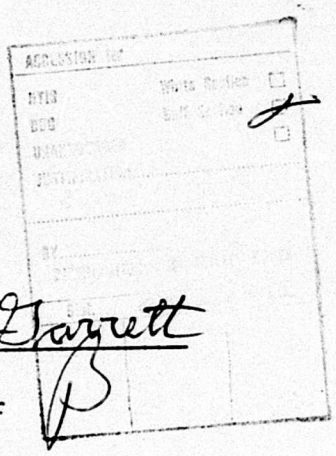

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FOREWORD

This report covers the work performed under Contract number F33615-72-C-1125, Project 505-1, for the period from May 1, 1972 to May 31, 1975.

The purpose of this contract with Fairchild Camera and Instrument Corporation, 464 Ellis Street, Mountain View, California, was to develop and implement the manufacturing methods and processes required to fabricate radiation-hardened TTL integrated circuits utilizing single and multilayer anodized aluminum interconnections; and to fabricate radiation-hardened multichip integrated circuit assemblies using aluminum beam lead and aluminum bump integrated circuit attachments to aluminum interconnections on a multilayer ceramic substrate in an hermetically sealed package. Mr. Jack Garrett, Air Force Materials Laboratory (LTE), Wright-Patterson Air Force Base, Ohio, is the Air Force Project Engineer.

Dr. C. J. Dell'Oca was the Fairchild Project Manager. The chief contributors to this program and to the preparation of this report are G. L. Adams, R. W. Marshall, F. S. Kovacs, D. K. Myers, and R. J. Kopp.

This report was submitted by the authors in July 1975.

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Investigations are described which lead to the implementation of manufacturing methods and processes for fabrication by aluminum anodization of single and dual layer metal interconnects for radiation hardened integrated circuits. In addition, an all aluminum, radiation hardened, multichip assembly method is described that completely eliminates flying wires and achieves a high chip packing density in a hermetically sealed package. These manufacturing methods are demonstrated by the fabrication of anodized radiation hardened integrated

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circuits and by the fabrication of a multichip six bit adder, each containing twelve anodized and/or inverter TTL gates and four anodized quad two input NAND gates.

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SECTION I
INTRODUCTION

Radiation hardened integrated circuits have lagged behind commercial circuits in the degree of complexity possible because of masking limitations imposed by the various dielectric isolation processes. Once the masking limitations of a process are reached, increased complexity can be achieved either by fabricating more complex monolithic circuits with multi-layer metallization or by fabricating hybrid multichip assemblies in which the complex function is obtained by interconnecting a number of monolithic circuits on a common metallized substrate. The two methods are not entirely independent in that the complexity that can be achieved in a multichip assembly of reasonable physical size is ultimately governed by the complexity of the monolithic circuits chips. Since the yield (ability to fabricate) of monolithic circuits drops rapidly with increasing complexity, it is necessary to develop: (a) Manufacturing methods which improve monolithic circuit yield, and (b) multichip assembly manufacturing methods which give high circuit packing density and which utilize low Z materials compatible with radiation environments. This report describes: (a) The development of manufacturing methods which will reduce the yield loss of radiation hardened monolithic circuits caused by a single or dual level metallization process, and (b) the fabrication of a radiation hardened six-bit adder by using a multichip assembly process which is reliable and fully compatible with radiation environments.

One of the major contributors to yield loss is the two level metal interconnect process required by complex monolithic integrated circuits. When the conventional metallization process is used, the first level of interconnections is formed by depositing aluminum on the circuit wafer and then delineating the pattern required by using photoresist masking and etching. The resulting sharp steps which occur in the surface topography at each metal line edge are detrimental to subsequent processes required for oxide insulation and second level metal formation. Consequently, after second level metal is completed, a percentage of wafers must be rejected for faulty metallization. These

wafers are lost because rework is not feasible at this point. As a result, etching techniques have been developed which give a more gentle contour to the sides of aluminum lines. However, slope etching techniques are difficult to control and at best provide only a partial solution to the problem.

A much better solution, which will be described in this report, is to use aluminum anodization to form the first layer metal interconnects. In this process, the required aluminum pattern is again masked with a layer of some material, however, instead of etching, the unwanted aluminum is now converted to an aluminum oxide insulator. The aluminum oxide now fills the space between the aluminum lines and the result is a surface topography free of sharp steps and thus very amenable to second level metal processes. In addition to improved yield, anodization also results in improved reliability. It has been shown, for example, that anodization markedly improves aluminum resistance to electromigration[1]. Another feature, is that anodization suppresses hillock formation[2]. Hillocks are thermally induced aluminum outgrowths on the surface of the first layer of aluminum. These outgrowths can interfere with subsequent passivation and metallization processes. Another benefit is that the aluminum oxide is hard and provides mechanical protection to the aluminum. This is important in that is prevents damage to aluminum lines during wafer fabrication and encapsulation.

Multichip assembly methods have been used for some time in applications requiring operation in radiation environments. The present systems suffer from several drawbacks. These assemblies generally utilize high Z metals for attachment and interconnections which are not reliable in radiation environments. The reliability is not as good as it might be because flying wire bonds are not altogether eliminated, the substrate is attached to a package and undesirable inter-metallics can occur. This report describes a technology which removes all of these drawbacks.

The multichip technology described herein utilizes an all aluminum metallization system for the substrate and for the integrated circuits.

Aluminum beam leads or aluminum bumps are formed on radiation hardened monolithic circuit chips and these chips are ultrasonically bonded to the substrate metallization. Thus unwanted intermetallics are avoided and low Z metals are used. In addition, the substrate utilizes two level aluminum metal interconnection and also forms the bottom of the hermetic package thereby entirely eliminating flying wire interconnections. Finally, the substrate metallization is formed by the same techniques that are used in the fabrication of monolithic integrated circuits providing for easy cross-overs and a high chip packing density.

SECTION II

ALUMINUM ANODIZATION PROCESS DEVELOPMENT

INTRODUCTION

Basically the task at hand was to develop a manufacturing process in which the aluminum interconnect pattern of radiation resistant integrated circuits is defined by anodization. Thus,it was necessary to:

- Develop masking processes which protect the required metal pattern during anodization.
- Develop anodization processes which result in adequate electrical isolation and clearing of aluminum between metal lines.

In addition, from a manufacturing point of view, it was required that a process be developed which would:

- Be compatible with other integrated circuit manufacturing processes (this is covered in Section III).
- Be relatively simple.
- Be amenable to multi-wafer processing.
- Be reproducible, i.e., provide good yield.
- Not affect, or better still, improve device reliability.

There are a large number of anodization conditions and processes as well as a number of masking materials and processes available which lead to a large number of possible anodization process sequences. While it was impossible to investigate more than a few of these, many

variations were eliminated because of our understanding of anodization and the resulting anodic oxide properties. In addition, the manufacturing requirements served to further limit the number of variations considered for investigation.

Since our understanding of the mechanism of anodization is important to defining and solving the present problem, a section covering the properties of anodization has been included. In addition, the discussion is enlarged upon in the various sections which present the various aspects of process development.

ANODIZATION

Anodization refers to the growth of an oxide on an electrode by causing the electrode to act as an anode in an electrolytic cell. A positive voltage is usually applied in order to grow oxides of substantial thickness. The anodic oxide film grows by mass transport of ions across the oxide under the influence of high electric field developed in the oxide by the applied voltage. For example, with aluminum, aluminum ions are transported from the metal across the oxide to the oxide-solution interface, where they combine with oxygen ions from the solution and cause oxide growth. Similarly oxygen ions can combine with aluminum to form new oxide at the metal-oxide interface. The fraction of oxide produced by transport of a given ion species depends on the material being anodized and the anodization conditions. Anodization conditions are defined as, the properties of the electrolyte (formulation, temperature, and agitation), the applied conditions (voltage or current), and the resulting conditions (current or voltage), the duration of the anodization, and for the application considered in this report, properties of the aluminum (roughness and purity).

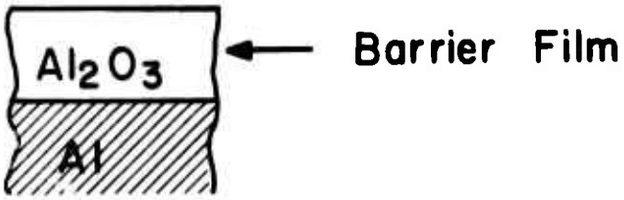
Two types of anodic oxide films of aluminum are distinguished, i.e., barrier and porous anodic oxides, and the anodization giving rise to these oxides is referred to in the same manner (Fig. 1). Barrier films are dense and are formed by anodizing in non-aggressive electrolytes such as near neutral ammonium tartrate or ammonium citrate solutions. Porous films are formed in more aggressive electrolytes which attack the oxide (Figure 1). The initial growth is essentially the same as that for barrier films, however, pores soon begin to form and eventually a point is reached where film growth is balanced by oxide removal at the base of the pores. The result is a barrier film interposed between the metal and a porous layer.

The anodic oxide film grows at the expense of the aluminum. That is, aluminum is used up or converted to an oxide. Calculations based on the density of the barrier layer and that of the aluminum, indicate that 1Å of aluminum produces about 1.65Å of aluminum oxide. The actual conversion can be less than this depending on loss of aluminum to the electrolyte. Barrier layers can only be grown to a thickness of about 5000Å; hence, they cannot be used for the conversion of aluminum in integrated circuits which is typically about 1μ in thickness. Porous films, on the other hand, can be grown very thick and hence can be used for metal delineation. In either case, however, the thickness of the barrier layer is fixed within narrow limits by the anodization voltage.

The properties of barrier films are, except for thickness, insensitive to formation conditions and hence any of the available barrier forming electrolytes work satisfactorily. For the present work, barrier films were formed in a stirred 3% tartaric acid $H_2(C_4H_4O_6)$ solution with pH raised to 5.5 with NH_4OH and the solution kept at 25°C.

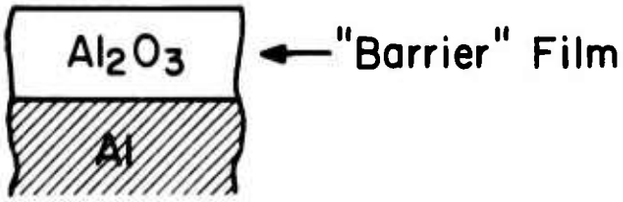
ALUMINUM ANODIZATION

A. Barrier Anodization



B. Porous Anodization

(a) Initial Formation



(b) Pore Initiation

(c) Porous Film Growth

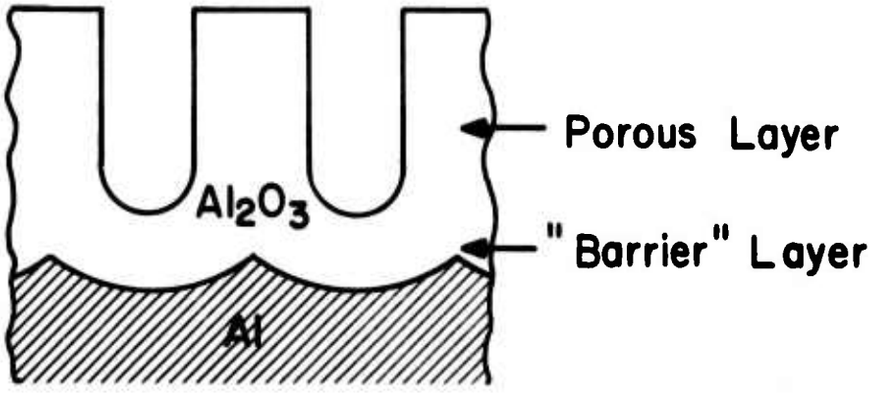


Figure 1 - Types of Alumina Formed by Anodization of Aluminum.

Under formation at constant current * (constant current forced into the cell) the film thickness increases linearly with time (according to Faraday's law) which requires the voltage to rise linearly with time to maintain the electric field in the oxide required for growth. At 10 mA/cm^2 applied current, the electric field is about 8.3×10^6 $volts/cm^{-1}$.

By comparison, the properties of porous films are highly dependent on anodization conditions; however, the formation characteristics are similar in form. At constant current formation*, the film thickness increases linearly with time. The voltage (see Figure 2) increases at first, but after perhaps passing through a short lived maximum, becomes constant when steady state is reached between etching at pore bases and film growth. That is, the voltage levels out at the value necessary to maintain the current across a barrier layer of fixed thickness. The voltage is referred to as the operating or steady state voltage.

Although there are many anodization conditions, the operating voltage serves as a common denominator in that pore diameter, pore wall thickness and barrier layer thickness are all directly related to operating voltage [4]. For example, the lower the voltage, the smaller these dimensions; thus, the greater the pore density, the lower the physical strength of the films. The question, therefore, is what controls the voltage? Of primary importance is the electrolyte; the more aggressive the electrolyte the lower the voltage for the same growth rates (see Table 2-1). For the same electrolyte, increasing temperature or as demonstrated in Figure 2, decreasing the applied current density decreases operating voltage.

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*Constant current conditions lead to natural steady state formation and hence are best understood.

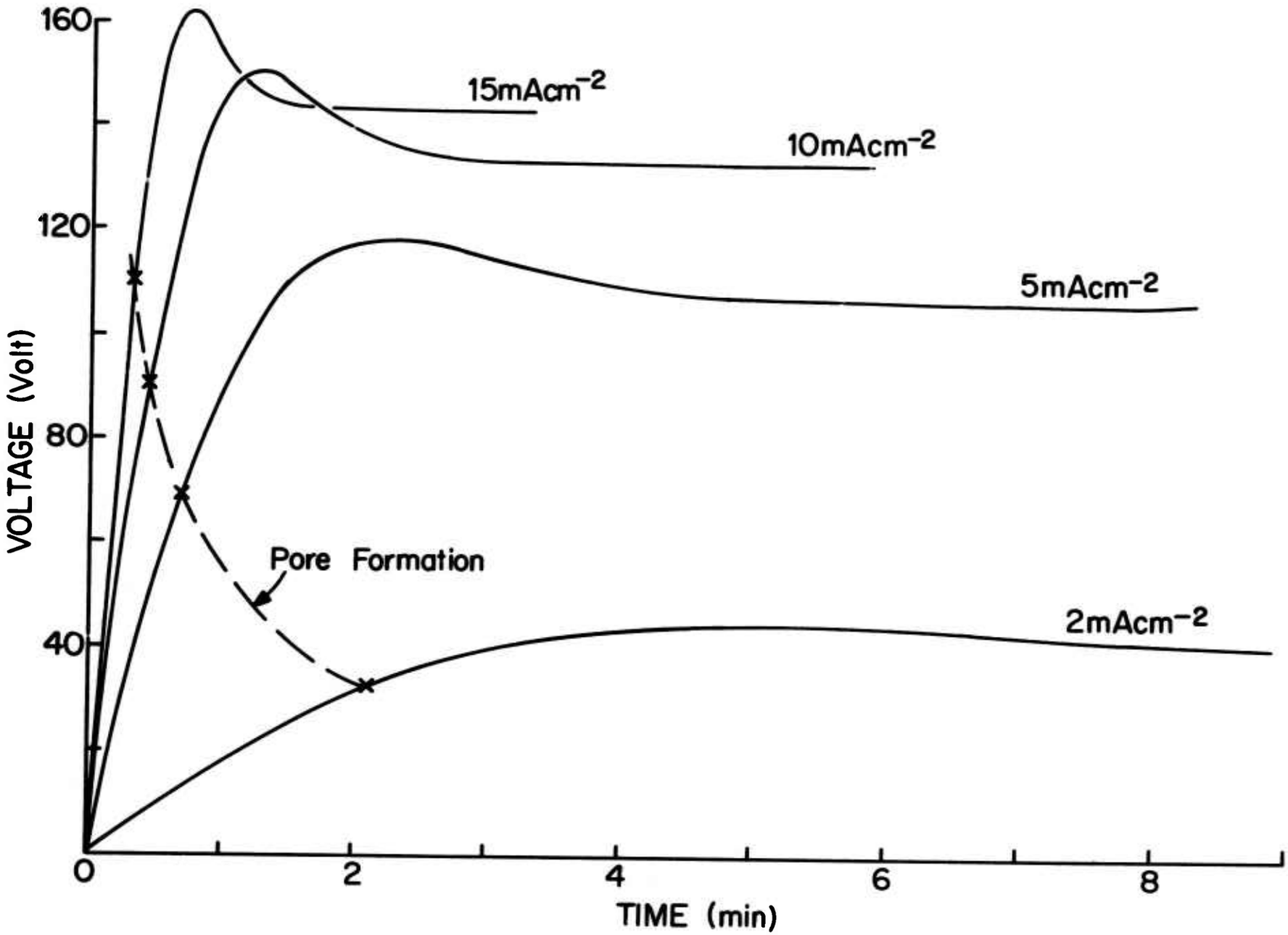


Figure 2-2 - Anodization characteristics for Porous Alumina Films grown in Dilute H_3PO_4 (Ref. 3)

TABLE 1

POROUS ANODIZATION AT 10 mA/cm^2 AND 25°C

	High Voltage	Low Voltage
Electrolyte	4% H_3PO_4	4% H_2SO_4
Operating Voltage	133 volts	20 volts
Barrier Layer Thickness	1500 Å	250 Å

METHODS OF INVESTIGATION

Test Vehicles

9708 AND-OR-INVERT Gate: Although the six-bit binary adder will employ both 9702 and 9708 radiation hardened integrated gate circuits, the 9708 was chosen for the initial process investigation. The 9708 was chosen because: (a) each 9708 die contains two resistors which may be tested independently and would therefore allow differentiation between resistor related and anodization related effects, and (b) it is possible to electrically test the quality of the isolation produced by anodization on each die. Figure 3 shows the 9708 die. The 9708 is a metal mask option of the 9705 gate circuit in which several resistors and transistors used for the 9705 are not utilized by the 9708. The resistors can therefore be measured independently from the rest of the circuit. The resistors are R_3 and R_4 and are respectively 520 ohms (2.6 squares) and 4000 ohms (20 squares). A thin film resistor test mask, the XRA was also used as a test vehicle and is described in Section III, under resistors.

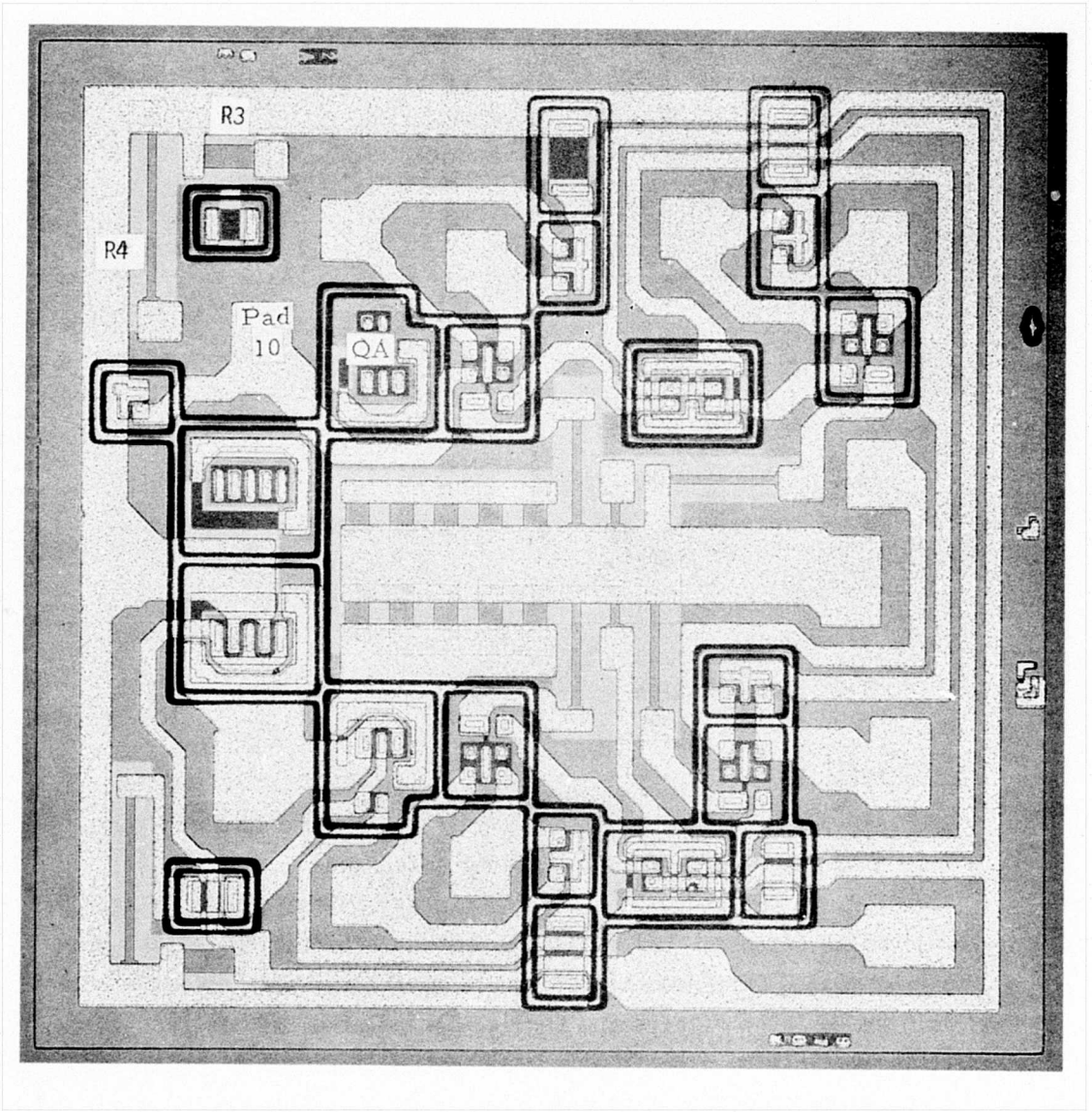


Figure 3 - 9708 And-Or-Invert Gate Circuit Die

The anodization isolation can be assessed by probing between the transistor marked A and pad number 10 in Figure 3. Transistor A is not part of the 9708 circuit and thus it is possible to apply high voltage between it and the adjacent line which is 1 mil away. The 9708 wafer also contains five test patterns which contain resistors on which anodization isolation and device properties can be evaluated. The ability to measure the same test parameters on each die provides information concerning parameter variations across a wafer.

Anodization Test Pattern: A special test mask set, designated as MASC, and specifically designed to test certain anodization features for single and dual layer metal has also been used in developing the anodization process. Figure 4 shows the first metal layer produced after anodization using this mask set. The closely spaced (0.2 mils) interdigitated fingers are specifically designed to test anodization isolation and check for metal bridging. Note also, that the metal extends along the scribe line. This metal is later removed, but initially it serves to distribute current to each die for uniform anodization across the wafer. It is also possible to compare directly the isolation of metal connected to the metal in the scribe line and the metal not directly connected. The significance of this will become evident later. The second layer metal will be described in the section which discusses dual layer metal anodization process development.

Anodization Procedure:

Manufacturing process development and evaluation was for the most part carried out using the single wafer anodization cell shown in Figure 5. The wafer on which the aluminum is to be anodized is held by a clothespin-like clamp in the electrolyte. This clamp is the

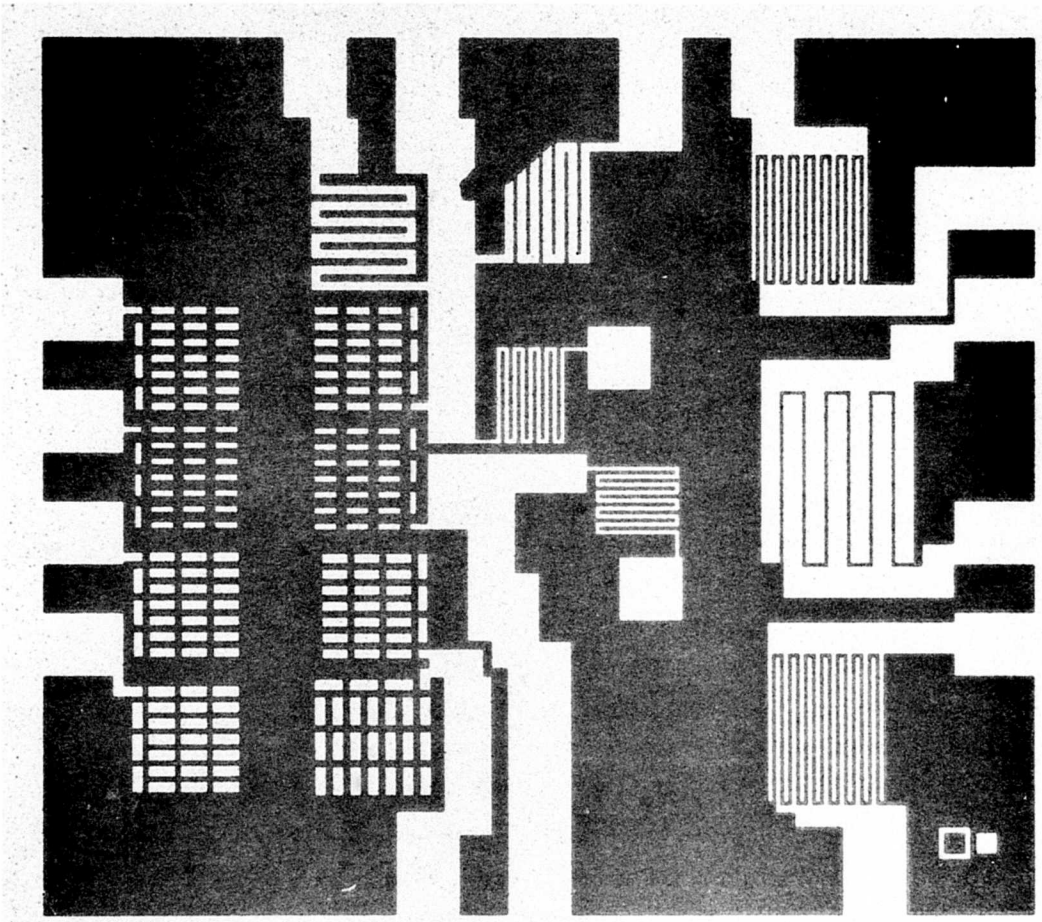


Figure 4 - The MASC Anodization Test Structure Showing First Level Metal After the First Anodization

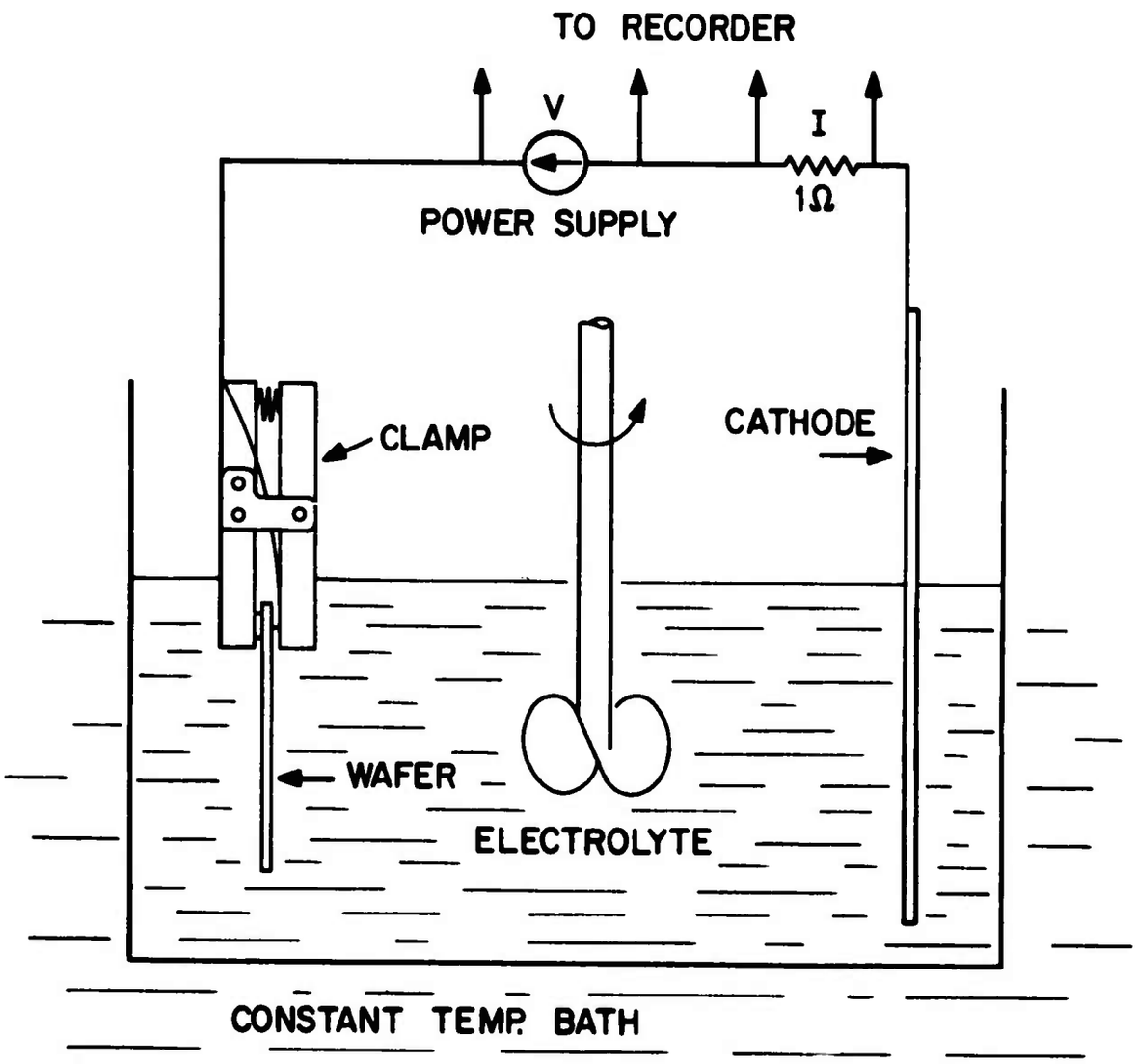


Figure 5 - Schematic Representation of the Anodization Cell in a Constant Temperature Bath. Current (Sampled Across a 1 ohm Resistor) and Voltage are Displayed on a Chart Recorder

forerunner of the multiwafer anodization fixture that was developed. Metal stubs in the jaws of this clamp hold, and at the same time, make electrical contact to the aluminum on the wafer. After a deionized water rinse, the clamped wafer is transferred to the anodization cell (Figure 5). The wafer is completely immersed in the electrolyte which is stirred and maintained at the required temperature by a constant temperature bath. An aluminum sheet serves as the cathode. Power is applied between the clamp and the cathode and the anodization is carried out. The anodization voltage and current are monitored by a two pen recorder and accurately displayed on a strip chart.

A typical process would be: deposit the aluminum on the test or circuit wafers; protect the required aluminum metallization: carry out the desired anodization, carry out any other process necessary and then perform the required tests and analysis on the wafer.

Anodization Conditions: The anodization conditions will be those which give the best results, but whenever possible, they were chosen for ease of manufacturability. Thus the temperature of the electrolyte was set at 25°C. This is slightly above room temperature and is fairly easy to maintain since power input into the cell generally raises its temperature. For the present investigation, the temperature was kept at 25°C in order to reduce the number of variables to be considered in the interpretation of results.

The anodizations were carried out at a constant applied current since this leads to steady state growth conditions which are most easily interpreted. However, an upper voltage limit was set which varied depending on the purpose of the anodization.

Barrier anodizations were carried out in a 3% (by weight) tartaric acid solution with pH adjusted to 5.5 using $(NH)_4OH$. A current density

of 10mA/cm^2 was used and the voltage was limited to less than 180 volts (typically 160 volts) because film breakdown can occur at above 200 volts. Citric acid was also used.

From our discussion of porous anodic oxide film properties, it is evident that in general the investigation can be limited to low and high operating voltage electrolytes. In this case a four percent solution of H_3PO_4 and H_2SO_4 was used to respectively achieve high and low operating voltage.

RESULTS

Anodization Masking

The required aluminum interconnects are formed by protecting them against the anodization which converts the unprotected aluminum to an oxide. Several materials have been evaluated in terms of their ability to provide this protection. These are photoresists, anodic oxides of aluminum and vapor deposited oxides of silicon. The requirements placed on these protective coatings is that they must be able to withstand the highest anodizing voltage (160 volts) without lifting or breakdown.

A successful photoresist process would involve the least number of steps and probably be most attractive from a manufacturing point of view. In general, however, it is necessary to develop special processing methods to improve the photoresist adhesion to aluminum and hence the resistance to lift during the anodization. Even with these precautions, photoresist formulations undergo subtle changes with time which require continuous redevelopment of processes. In addition, the performance of a photoresist is affected by environmental factors and aluminum surface properties. These little understood effects lead

to changes in performance almost from day to day. For these reasons, it was concluded that photoresist would not provide a reliable continuous high yield process. However, it should be mentioned that of the photoresist tested, Hunts-G-Line worked quite well even at the high voltages used here (160 volts); but in some cases, lifting, or some anodization of the underlying aluminum occurred. However, it should be pointed out that photoresist performance improves with decreasing voltage of anodization and therefore would be more reliable at lower anodization voltages. However, it will become evident that lower voltages are less desirable.

Dielectric masking layers require additional processing steps since the overcoat must be formed and then defined by photoresist masking and etching. However, they are capable of reliably withstanding the high applied voltages of anodization and therefore give rise to reliable line definition. Two types of dielectrics have been investigated. The first is a vapor deposited oxide of silicon(PVx) which is commonly used over aluminum metallization and therefore the processes required for delineating this material to the aluminum pattern are well known. This oxide is produced by the oxidation of silane at $400^{o}C$. Tests indicate that a thickness of 3000 Å is more than sufficient to mask against anodization voltages of up to 180 volts. The second dielectric is formed by anodizing the aluminum. This could be a barrier or a porous anodization. In either case, the anodizing voltage reached in forming these layers must exceed by a certain margin the voltage which is used in the anodization for delineation. To be more precise, for proper protection, the electric field applied during delineation must be less than the final electric field reached in the formation of the protective film. The margin required depends on the duration of anodization since the protective layer is being attacked by the electrolyte at a rate dependent on electric field, the thickness decreases to a point where appreciable current begins to

flow and porous anodization begins in the protected area. For the anodizations developed in this program, it was found that a 25 volt margin was more than sufficient.

The process sequences used with the above protective layers starting after aluminum evaporation are:

(a) Photoresist Mask
- Form photoresist pattern of aluminum metallization
- Porous anodize

(b) (PVx) Mask
- Deposit PVx
- Mask and etch PVx to metal pattern
- Porous anodize

(c) Al_2O_3 Mask
- High voltage barrier (2500Å) or porous (~3500Å) anodization
- Mask and etch Al_2O_3 to metal pattern
- Porous anodize at lower voltage

(d) Al_2O_3 and Photoresist Combination
- Cover unwanted aluminum areas with photoresist
- High voltage barrier or thin porous anodization
- Strip resist
- Lower voltage porous anodization

All of the foregoing processes have been investigated and found feasible on a manufacturing basis. Process (a) is the simplest but also least reliable. Process (d) uses photoresist to prevent

anodization of the unwanted aluminum while the required pattern is being protected. This is somewhat better than (a) since some anodization under the photoresist can be tolerated, although it may result in non-uniform delineation properties. Process (b) and (c) are essentially equivalent and give excellent manufacturing reliability. each has some advantages which will be discussed under dual layer metal anodization process development. For single level metal anodization, the SiO_2 passivation was preferred because the process is well known and because the highest anodization voltage can be used.

Anodization Characteristics:

Typical anodization characteristics obtained from the anodization of circuits or test patterns are shown in Figures 6 through 8. These characteristics are called anodization curves and show the time development of current and voltage during the anodization. In these results a constant current density of about $10mA/cm^2$ of aluminum area to be anodized is applied and the voltage limited to some desired value. Figure 6 and 7 show the case where the limiting voltage is set above the peak voltage. In these cases, as anodization proceeds the voltage rises to a peak of about 21 volts for 4% H_2SO_4 (Figure 6) and 154 volts for 4% H_3PO_4 (Figure 7). The voltages then settle out at a somewhat lower value which signifies a steady state condition between the conversion of aluminum to oxide and the etching at the base of the pores in the oxide. This point is defined as the operating voltage or steady state voltage. Eventually the remaining aluminum is thinned to a point where it becomes increasingly resistive and the voltage now increases in order to pass the current. The voltage increases to the previously set limiting value and remains at this value. At the same time, the current decreases rapidly and levels out at a low value which indicates that the anodization is complete; that it, all of the aluminum has been converted to an oxide. This usually occurs in

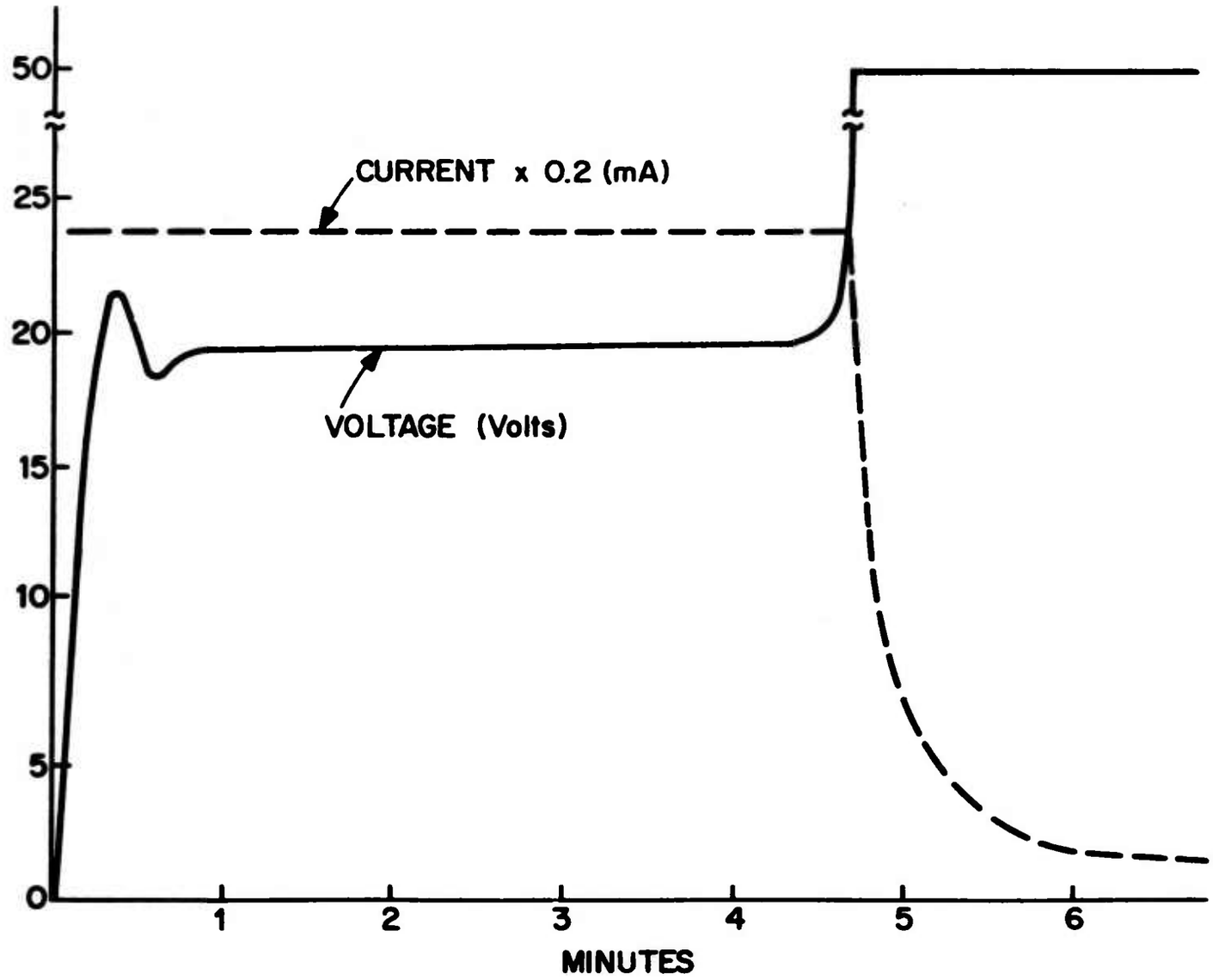


Figure 6 - Typical 9708 Wafer Anodization Characteristics in 4% H_2SO_4 at 25°c

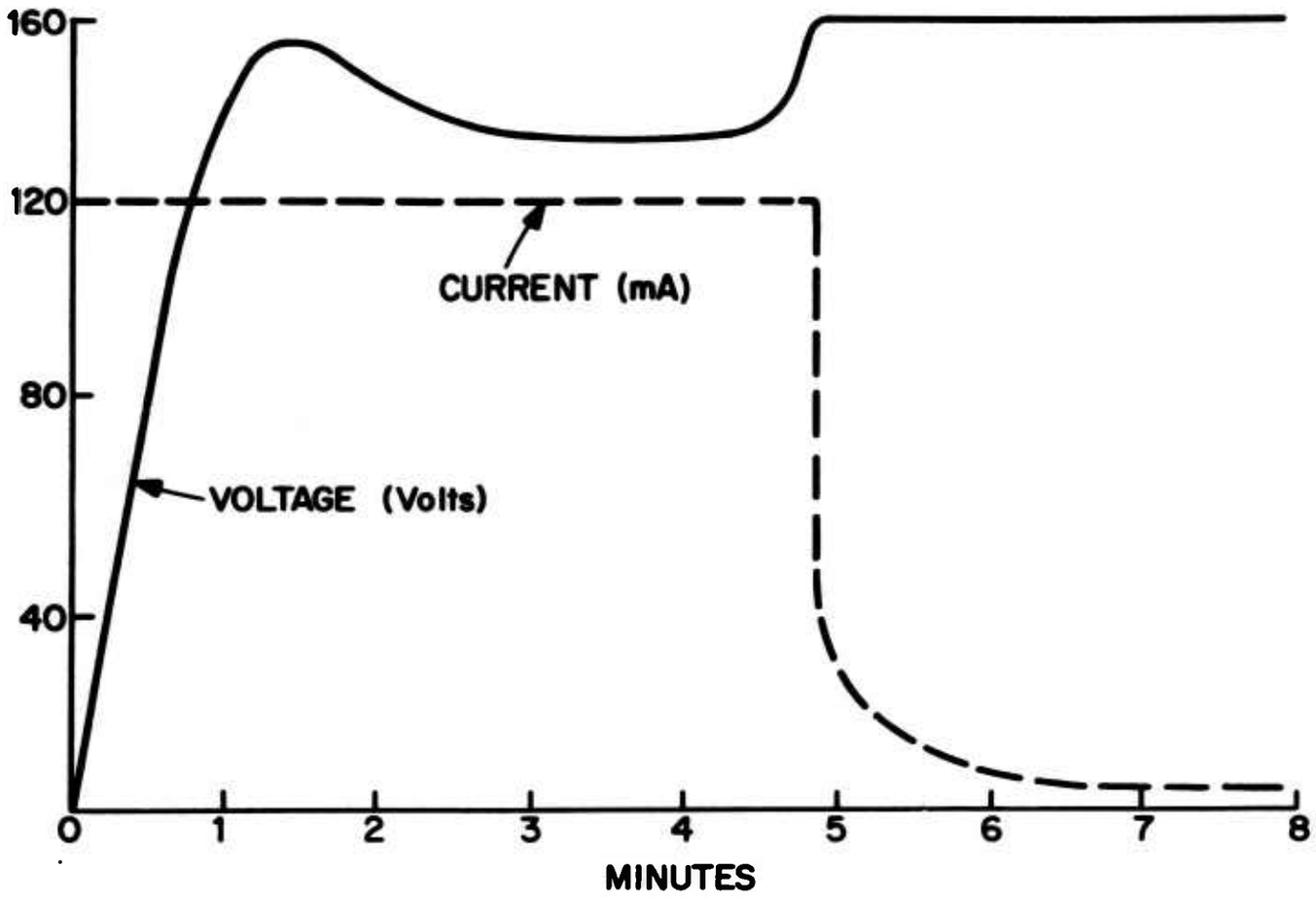


Figure 7 - Typical 9708 Wafer Anodization Characteristics in 4% H_3PO_4 at 25°c

about six minutes for aluminum of about 1μm thickness.

In the case where a high voltage thin porous layer or barrier layer is used as an anodization mask, the voltage is generally limited below the steady state voltage. Figure 8 shows a $10mA/cm^2$ porous anodization limited to 120 volts. The protective layer on the metallization was a 160 volt barrier anodic oxide. In the anodization, the voltage rises until it reaches the limiting voltage value and then is held constant. At this point the current decreases, eventually passes through a minimum and then settles out below the starting value at roughly the current density for which the limiting voltage is the steady state value. Again the end of the conversion is signified by a decrease in current to a low value. Note that because of the decreased current density, the anodization takes appreciably longer to complete.

The anodization characteristics are normally reproducible from wafer to wafer, although they can be significantly altered by aluminum quality, as will be discussed. However, for good quality aluminum, variations do occur in the manner by which the current decreases towards the end of the anodization cycle. Some wafers will have a current which drops off very rapidly, while in others it may be prolonged for several minutes. Thus, to insure complete anodization and to specify a manufacturing process independent of the variation in current decay, all wafers are anodized for twelve minutes. This specification has proven to be satisfactory.

DELINEATION CHARACTERIZATION AND OPTIMIZATION

Aluminum delineation regardless of how it is achieved may be characterized as to:

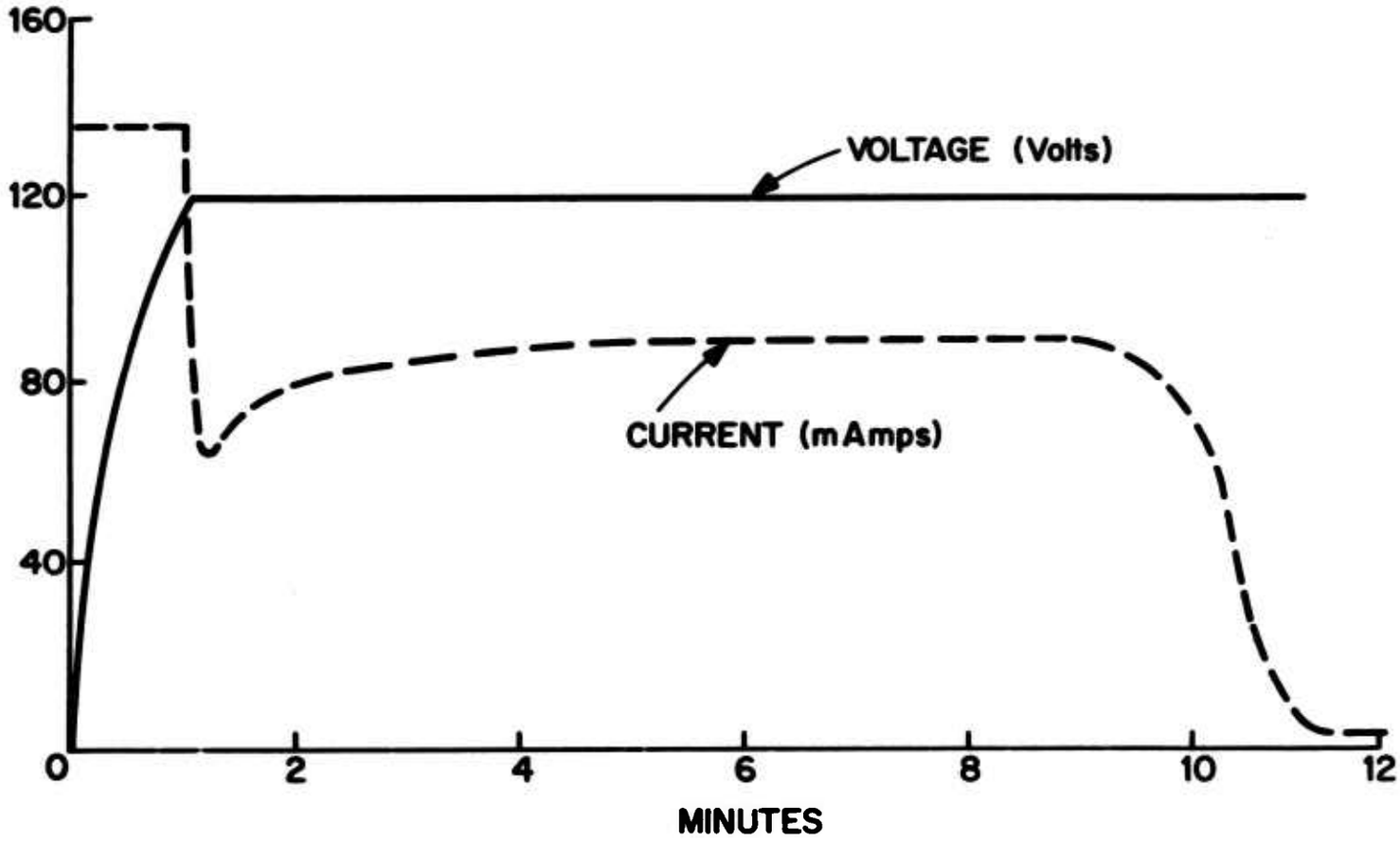


Figure 8 - Typical Anodization Characteristics in 4% H_3PO_4 for Test Structures Where Voltage is Limited Below Operating Voltage For Original Applied Current

- Line definition
- Aluminum clearing
- Electrical isolation

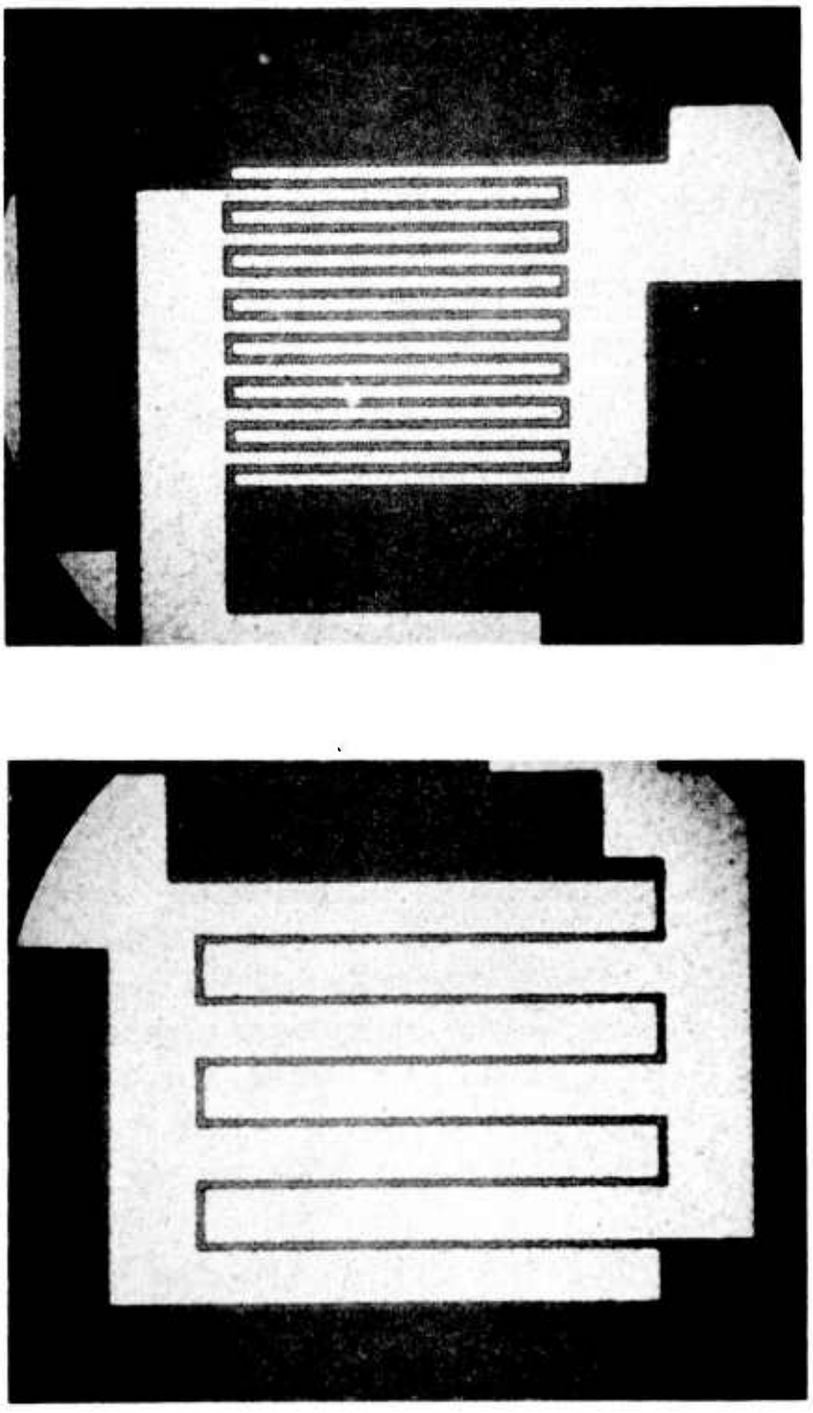
Line Definition

Line definition pertains to the ability to produce a metal pattern to a given specification. That is, certain tolerances must be maintained as to line width and spacing. The mechanism of anodization implies that the delineation of a line is only as good as the delineation of the masking material protecting the line during anodization. In general, however, it is well known that a thinner masking layer such as the vapor deposited oxides can be delineated by standard photolithography and etching much better than the thicker aluminum. What this implies is that the delineation of aluminum by anodization should be better than that obtained by standard etching techniques. This has been qualitatively observed: For example Figure 9 shows that a line width and spacing of 0.2 mil can easily be achieved by anodization. These results are for an SiO_2 masking layer about 3000Å thick. However, they are essentially unchanged for a 2500Å, Al_2O_3 barrier layer mask. Examples of the delineation of radiation resistant circuits are also presented in the following section on clearing and isolation.

The cross section of the aluminum lines will be described later, since this is significant to dual layer metal circuits.

Clearing and Isolation

Anodization is an electric field activated process. That is, for a given current density the anodization proceeds uniformly over the



(b) 0.2 mil Line Spacing

Figure 9 - Anodization Delineation of Aluminum On MASC Test Pattern

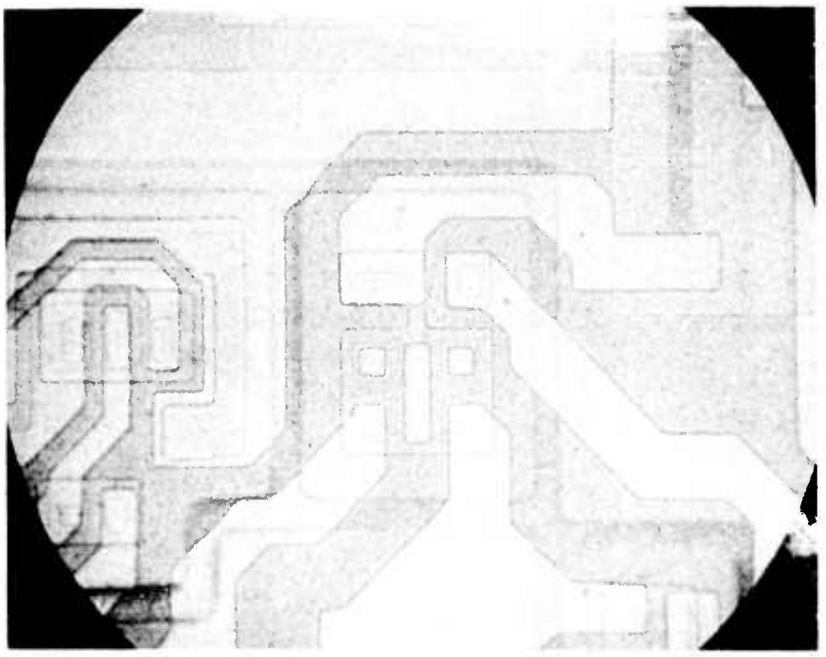
aluminum on the wafer until current conduction through the thinning aluminum layer becomes the limiting factor rather than conduction through the barrier portion of the porous film. Taking this into consideration, clearing will be affected by surface roughness and aluminum non-uniformity. Surface roughness results in localized unanodized aluminum particles left behind at the end of the anodization. Clearing refers to the extent to which the microscopic aluminum islands (referred to as "snow") occur. Aluminum non-uniformity may lead to incomplete electrical isolation. This is easily overcome,and in general, the anodization process leaves behind only aluminum islands, which are isolated from each other. If they were not, anodization would continue until isolation occurs. For this reason, electrical isolation does not necessarily imply good clearing, however, the converse is always true. The following section will enlarge upon the discussion in this paragraph and discuss the processing methods which achieve the best clearing.

Electrical isolation between adjacent aluminum lines was assessed by probing and measuring the current resulting from an applied voltage which was slowly raised to 300 volts. For the 9708 circuit, probing was done between pad ten and the metallization of the nearby electrically unconnected transistor "QA" (Figure 3). In the MASC test pattern. the isolation was assessed between interdigitated test structures such as the ones shown in Figure 9. Typically anywhere from five to twenty isolation evaluations were made at random per wafer tested. In general it was found, even in cases where clearing was poor (this is discussed later), that the isolation was good. That is, the measured leakage current at above 200 volts was generally less than the sensitivity of our instrument or about a nanoampere. This is to be expected since aluminum oxide is a good insulator.

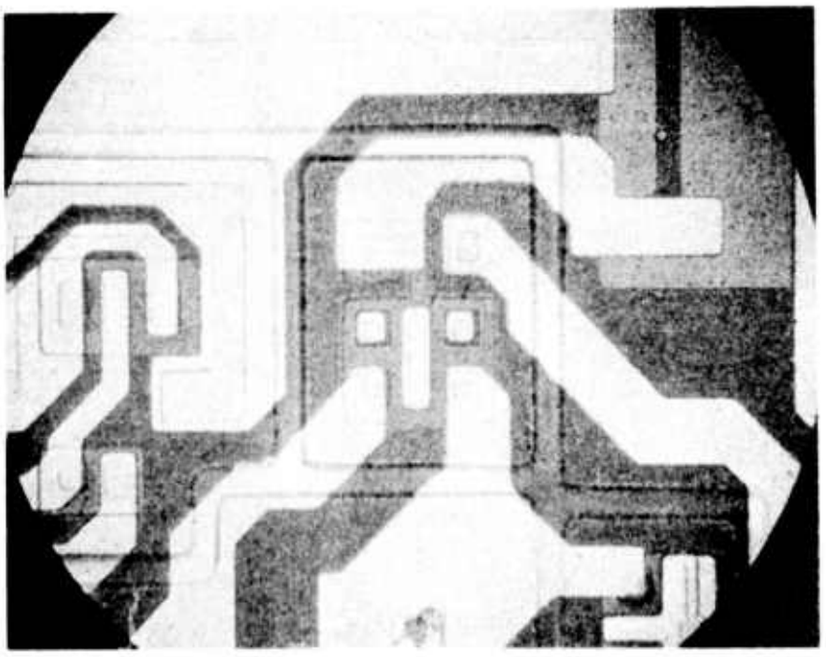
Effect of Voltage on Clearing: All else being equal, the higher the anodization voltage the greater the degree of clearing expected because higher electric fields are developed across regions that begin to isolate, and hence, the final isolation region is larger or the extent of "snow" less. This is dramatically demonstrated in Figure 10 and 11 which compare typical results from wafers processed in exactly the same manner and anodized under the same conditions in two different electrolytes. The basic difference between these two electrolytes was that the operating voltage of 4% H_2SO_4 is 20 as compared to about 134 volts for the 4% H_3PO_4. These results are supported by anodization carried out entirely in 4% H_3PO_4 at current densities which gave operating voltages of 45, 80, 108, 133 and 144 volts. A definite improvement with operating voltage was observed. The limiting voltage may also play a role in clearing, however, a high limiting voltage does not produce clearing equivalent to that obtained from a high operating voltage. In general, the limiting voltage is set 10 to 30 volts above the operating voltage.

Aluminum Quality and Clearing: Perhaps the most important factor in clearing is aluminum quality. Quality refers to surface roughness and aluminum purity. For this program, the aluminum was deposited by electron beam evaporation of 99.999 aluminum at pressures between 2 and 5 X 10^{-6} torr. During deposition the wafer may be heated to about 350^{o}C (referred to as hot substrate deposition) or may be unheated (referred to as cold substrate deposition).

The smoothest surface occurs for cold substrate aluminum since heating the aluminum causes grain growth and resulting surface roughness. Anodization of cold substrate aluminum results in the least snow which, in some cases, can only be resolved at magnifications of 400X and above. However, one of the drawbacks of cold substrate deposition is that non-uniform deposition occurs over oxide steps because of shadowing.

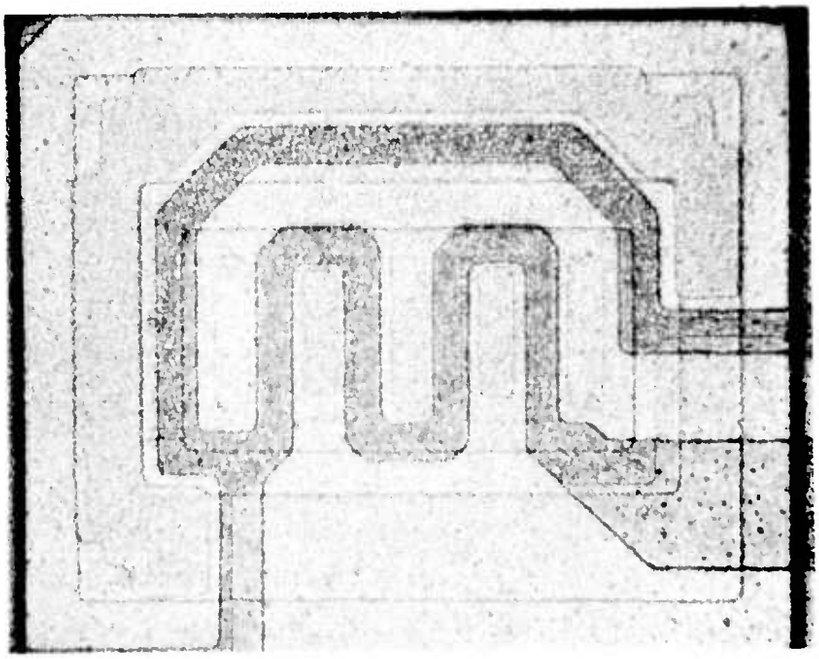


(a) Anodized in 4% H_2SO_4

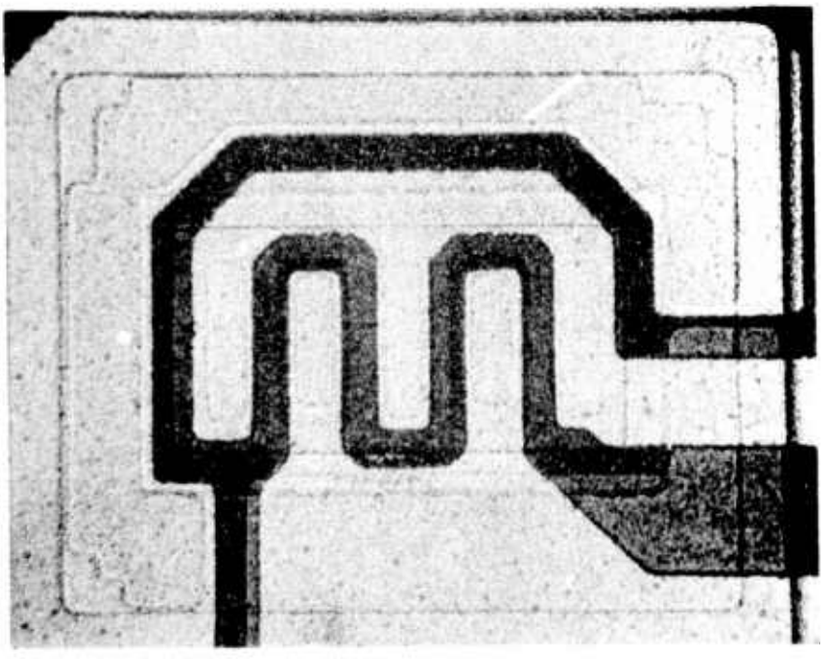


(b) Anodized in 4% H_3PO_4

Figure 10 - Comparison of Aluminum Clearing on Input Transistors of the 9708 Circuit (Magnification 250X).



(a) Anodized in 4% H_2SO_4



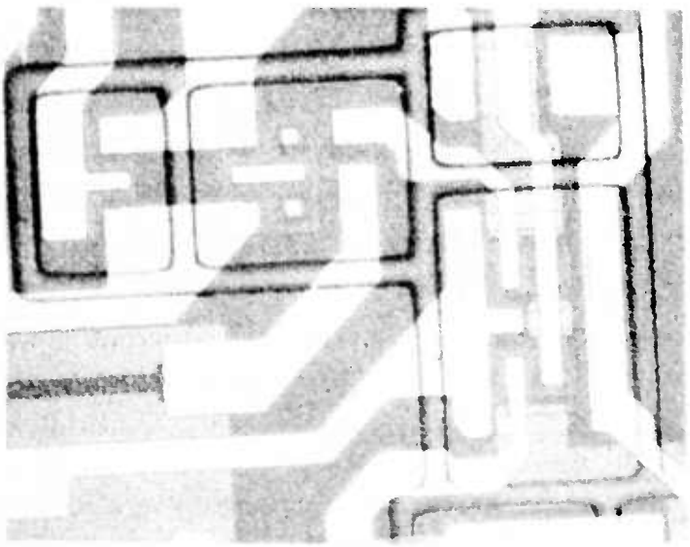
(b) Anodized in 4% H_3PO_4

Figure 11 - Comparison of Aluminum Clearing Between Transistor Emitters for a 9708 Circuit (Original Magnification 500 x)

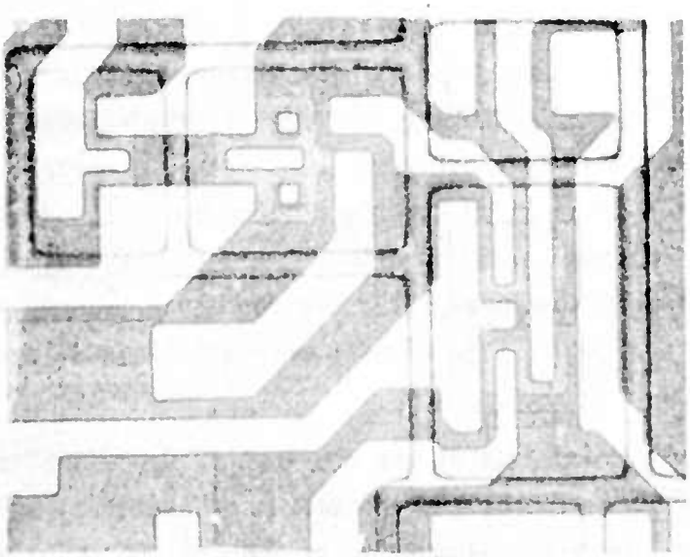
The result is that the aluminum is thicker at the top of the step and thinner along the side and near the bottom of the step and this gives rise to bridging after anodization. That is, complete clearing does not always occur near the top of the step and the result is a fine aluminum conducting bridge between aluminum lines running over the same step. As described later, this drawback may be circumvented at the expense of added process steps.

Hot substrate deposition covers steps more evenly and hence does not suffer from this drawback. However, hot substrate aluminum is inherently rougher and results in a greater degree of snow. In this case the clearing is better for lower deposition pressures because this results in smaller grain size. Figure 12 shows a comparison of clearing of aluminum deposited at the same rate but at different pressures. In each case the substrate was heated. It can be seen that the aluminum deposited at lower pressures ($\approx 2 \times 10^{-6}$ torr) gives the best clearing. Compare for example, the appearance of the resistor in the lower left hand corner of each photograph, only at the lower pressures can it be clearly discerned. This result is consistent with improved clearing from decreasing grain size. This, in fact, was the reason that except for the foregoing experiments, all aluminum has been deposited at the lowest pressure achievable with available equipment.

The roughness of the aluminum surface depends not only on deposition, but also on subsequent processing at elevated temperatures. In particular, the vapor deposition of SiO_2 is carried out at about 400°C and this causes grain size increase as well as hillock growth. The situation is far worse for cold than hot substrate aluminum because surface roughening is a function of the temperature difference between aluminum deposition and subsequent thermal cycling. On the other hand, anodization masking being a low temperature process does not change the surface properties. Thus for cold substrate aluminum, the best results are obtained using an anodic oxide anodization mask. However, for hot substrate aluminum the difference between using SiO_2 and Al_2O_3 was not



Deposition Pressure Approximately 0.2×10^{-5} torr



Deposition Pressure Approximately 2.0×10^{-5} torr

Figure 12 - Comparison of Aluminum Clearing for Aluminum Deposited at the Same Rate but at Different Bell Jar Pressures (Magnification ≈200X).

found to be significant.

On occasion it was found that the aluminum did not clear very well, and in some cases could not be anodized. In each case the problem was traced to electron beam evaporator malfunction. Through this, it was found that the shape of the anodization curve serves as a good indication of the aluminum quality. In all cases, if the shape is normal, such as that shown in Figure 13, the clearing is satisfactory. An abnormal anodization is shown in Figure 14. Note the difference in the current development with time in this figure. In this case a cable inside the evaporator had burned out during deposition. The resulting aluminum took almost twice as long to anodize and electrical isolation could not be achieved. Thus the anodization curves provide a good method of assessing aluminum quality for anodization.

Scanning Electron Microscope Observations: Direct observation of aluminum clearing ("snow") was also made using scanning electron microscopy (SEM). With SEM it is possible to examine the snow directly at high magnification. This is done after removing the aluminum oxide between the metal lines with a selective etch. The etch solution consists of 2% by weight Cr_2O_3 crystals and 5% H_3PO_4 in water @ 65°C. The etch time was 15 minutes, which should be sufficient to remove the porous oxide formed, although, it has been noted at times that the etchant does not completely remove the oxide after a heat treatment. However, this etchant does not attack aluminum, a property required for the present observations.

Although, the surface features of circuits produced by anodization will be extensively evaluated later, Figure 15 presents a typical micrograph obtained from circuits processed by anodization using a PVx anodization mask. In general, the anodic oxide exhibits a smooth surface of finer structure than the vapor deposited oxide covering the aluminum. Note the planarity of the surface. Figure 16 shows a

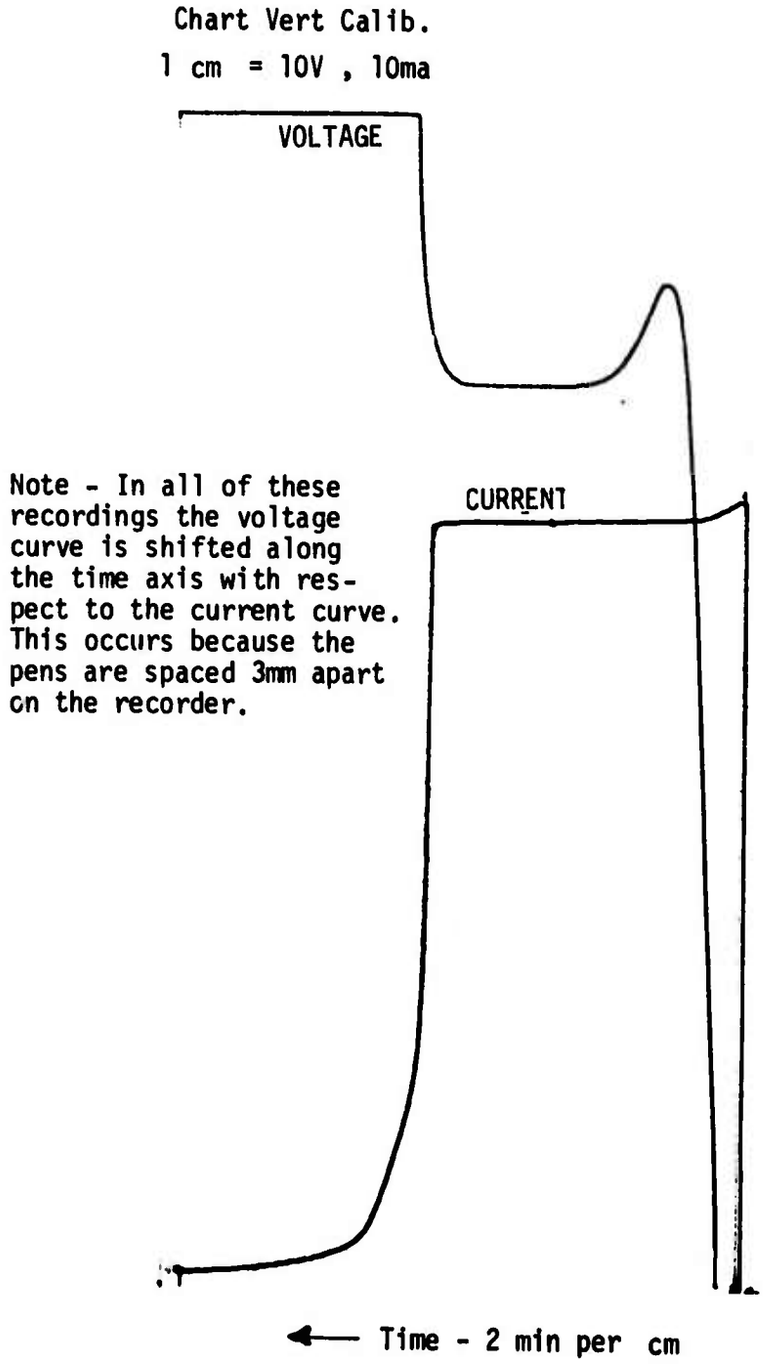


Figure 13 - Normal anodization curve.

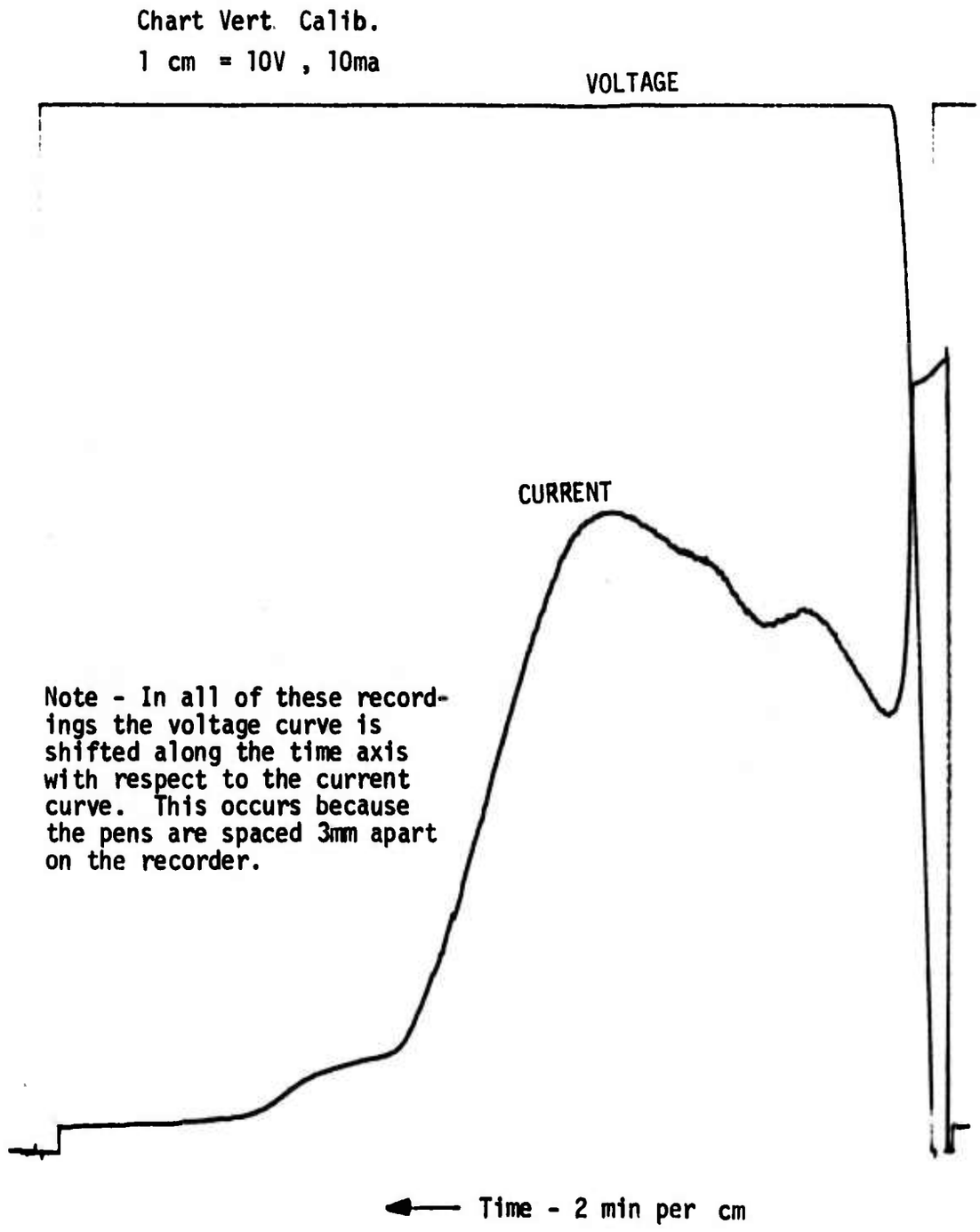


Figure 14 - Abnormal anodization curve.

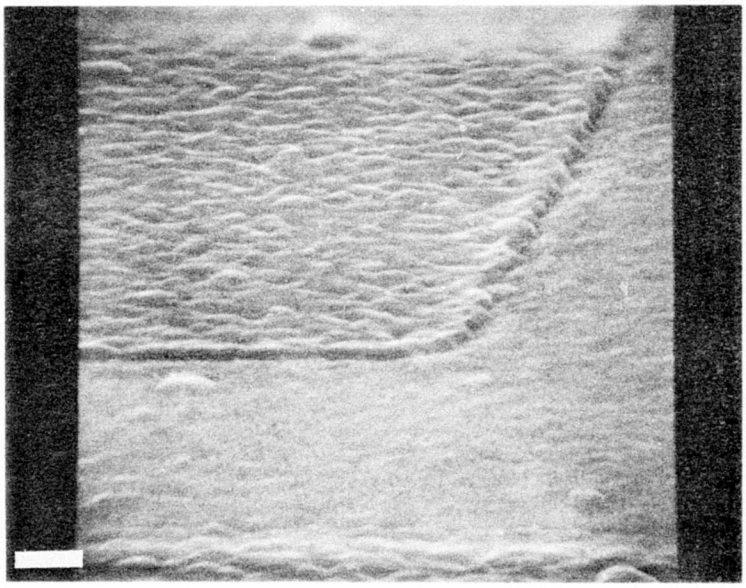


Figure 15 - Typical SEM Micrograph of an Anodized Aluminum. Vapor Deposited Oxide is Rough Area in Upper Left of Figure. Anodic Oxide is the Finer Structure. (White Bar at Lower Left is 2μm).

partially etched anodic oxide. The pores have been etched sideways and appear as fine standing filaments which collapse on further etching.

After the aluminum oxide is removed, the pore bases can be clearly seen on the sides of the aluminum lines. The sides appear as a mat of hollows (Figure 17) which represent the base of the pores formed during anodization. In examining these structures and others at higher magnification, it appears that the pore bases in the aluminum are about the diameter which, according to Sullivan and Wood[4], are expected from this type of anodization (4% H_3PO_4 @ 10 mA/cm^2).

The pore bases occur well up near the edge of the vapor deposited oxide mask. Since the anodization proceeds a small distance under the oxide, the pores must bend around the oxide ledge. The distance that the anodization proceeds inward is less than downward (being about 50%) since the aluminum oxide thickness is about fifty percent greater than the aluminum it displaces. Thus the upper edge of the aluminum line is under the oxide, however towards the bottom, the line gently curves out past the masking edge. Optically, this appears as a halo in the proximity of the aluminum line.

The density of snow is usually greater at the top or bottom of oxide steps, e.g., see upper photograph in Figure 17. Figure 18 shows the snow between metal lines at high magnification of the dark area. The darkening occurs because Figure 18 is a composite of SEM pictures taken of the area. In taking these pictures, the oxide under the SEM electron beam charges up and thus appears darker. At the higher magnification, the "snow" is readily apparent. In general, the snow particles are around 0.1μ in height. It can also be seen that a continuous electrical path does not occur. Areas somewhat better or worse than that shown in Figure 17 are probably representative of what has been achieved with the present anodization process. Nevertheless, in all cases presented, full electrical isolation is achieved between metal lines.

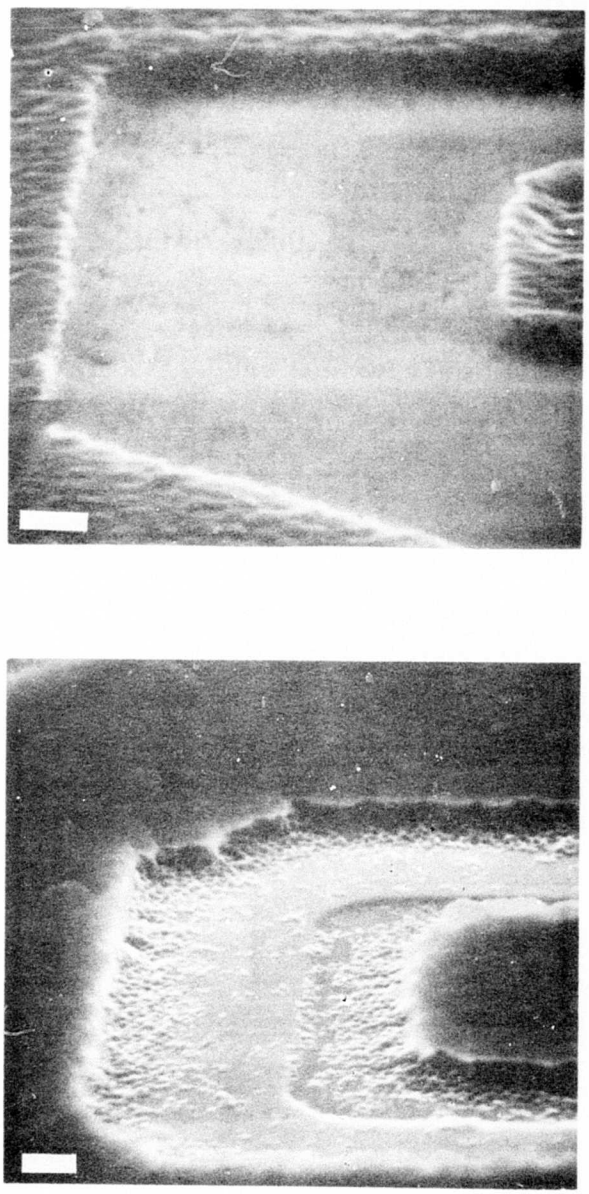


Figure 16 - Upper-micrograph of partially etched Al_2O_3 between device fingers (white bar is 2μm).
Lower-typical micrograph of similar area after Al_2O_3 removal (white bar is 2μm).

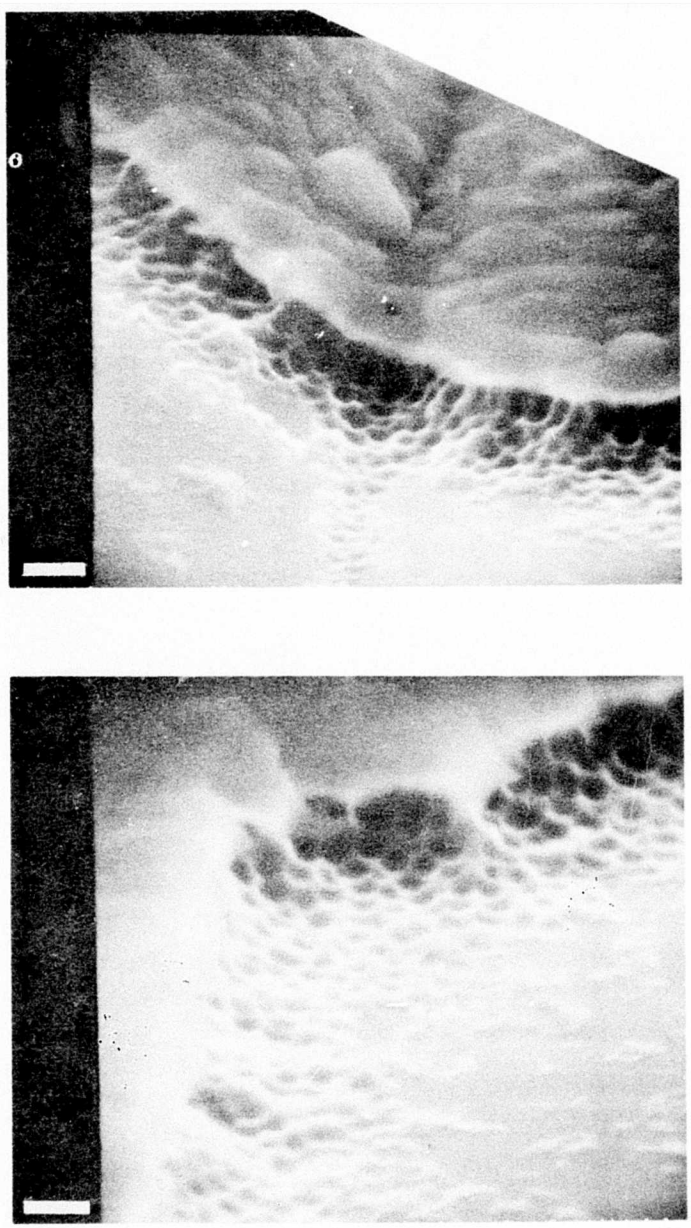
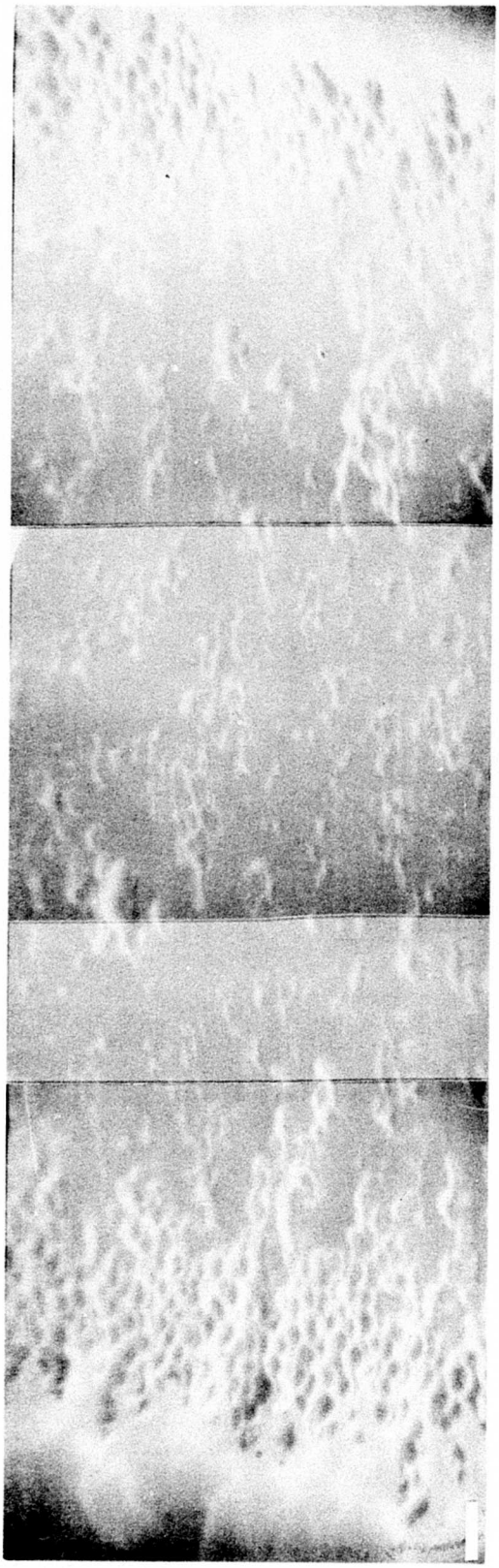


Figure 17 - Appearance of sides of metal lines showing pore bases after etching the anodic oxide (white bar is 1μm).



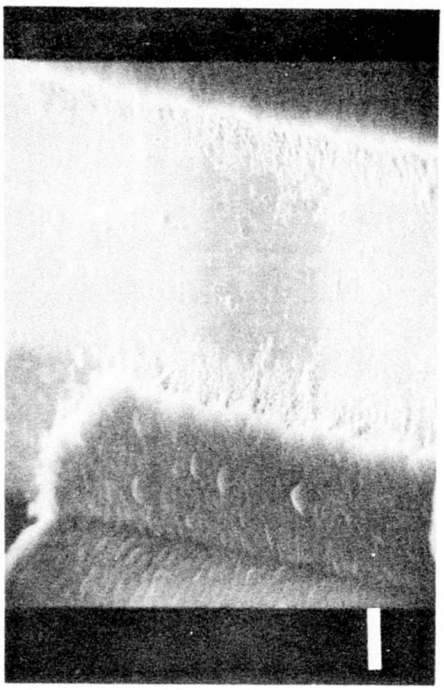


Figure 18 - High magnification (white bar is 1μm) observations of snow left after anodization of area which appears darker (due to charging in lower photo; white bar is 5μm).

Methods of Achieving Uniform Anodization and Clearing

The discussion thus far has implied that the anodization is uniform over the entire wafer. This is in fact the case: all wafers anodized in this program have, except for isolated cases, anodized to completion over their entire area. The isolated cases were caused by poor quality aluminum as discussed in the previous section or by insufficient removal of the vapor deposited oxide used for the anodization mask.

In general, when anodization is carried out from a single electrical contact, as is done in our case, complete aluminum conversion over the wafer surface should be the exception and not the rule. This is because to any point on the aluminum there is a voltage drop in the aluminum film which is different depending on the distance from the electrical contact. This voltage drop reduces the voltage available for anodization at any point on the wafer, hence the anodization rate will decrease away from the contact. This effect can, for the most part, be counterbalanced by using a high resistivity electrolyte and tilting the wafer such that the point contact is farthest away from the cathode. This forces the regions away from the clamp to anodize most rapidly; however, this is only a partial solution because the deposited aluminum films are non-uniform and will sporadically give rise to incompletely anodized areas.

The solution to this problem is not to develop more elaborate electrical or anodization contacting methods, but rather to develop methods of distributing the anodization current across the wafer particularly near the end of the anodization cycle. This has been achieved in two ways. One way utilizes the scribe line between die as a silicon conductive grid encompassing the entire surface. Another way utilized a purposely formed aluminum scribe line conductive grid.

Scribe Line Conducting Network: The original purpose of the scribe line was to define the integrated circuit die boundary and provide a convenient, oxide free area for scribing wafers into die. During the various device processing steps, the scribe line is open and the exposed silicon receives a number of diffusions which makes it fairly conductive. In order to use the scribe lines as a conductive path, it is cleared of oxide at the same time the contact cuts are opened to the active device areas. The aluminum, that is later deposited, contacts the silicon in the scribe line. The scribe lines come into play as the anodization nears completion, at this point, even though the scribe lines are resistive, they still serve to carry currents to those areas on the wafer which would otherwise become electrically isolated and not be anodized to completion.

Anodization of aluminum on a p-n junction isolated circuit wafer is simpler than on radiation hardened circuits because the bulk of the wafer, as well as the scribe line can carry current. In fact, current can flow from the bulk through the active device to the aluminum and hence, there is a direct contact to all metal lines on the die which ensures clearing. Granted, some of the junctions may be in a reversed bias condition, however;

a) The voltage used is generally sufficient to breakdown any reverse biased junction, and
b) The current required for final clearing is so small that junction leakage current, is probably sufficient.
c) With a direct conducting path to the lines, it is possible to over-anodize. Over-anodization results in reduction of line widths.

With dielectrically isolated devices, no current can flow from the bulk through the devices, however, all that is necessary is for current to flow from the scribe line to one of the aluminum lines on the die. From here, current can be carried to all parts of the die because all lines are electrically interconnected either through resistors or devices. Thus, unless the initial thickness of the aluminum is greater in the center than on the periphery of a die, anodization should go to completion over the entire die. This has been the case.

Aluminum Scribe Line Grid Connected to Metalization: In the second approach, the metallization mask is modified such that aluminum is retained in the scribe line during anodization and in addition, connections are made to the circuit metallization. Note that in this case, the scribe line and the metal connection must be protected from being anodized by covering them with SiO_2 as is done to the metallization pattern. This requires additional steps, since after anodization the connection to the scribe lines and remaining aluminum in the scribe line must be removed by a subsequent masking and etching operation. Figure 19 shows a 9708 circuit option with the scribe line connected to the metallization. The connection is made at the upper left hand corner and at the bottom center. Similar metallization mask options were designed for the 9702 circuit. The MASC test pattern did not have any exposed silicon scribe lines and for this reason used the metal scribe lines and connections.

Connection of the scribe line ensures the best possible clearing and complete isolation because now there is a conducting path from the clamp to all aluminum lines on the die. While it is now possible to over-anodize the lines with this method, it does remove the metal bridging at oxide steps encountered with anodization of cold substrate deposited aluminum. With hot substrate aluminum, it was found,

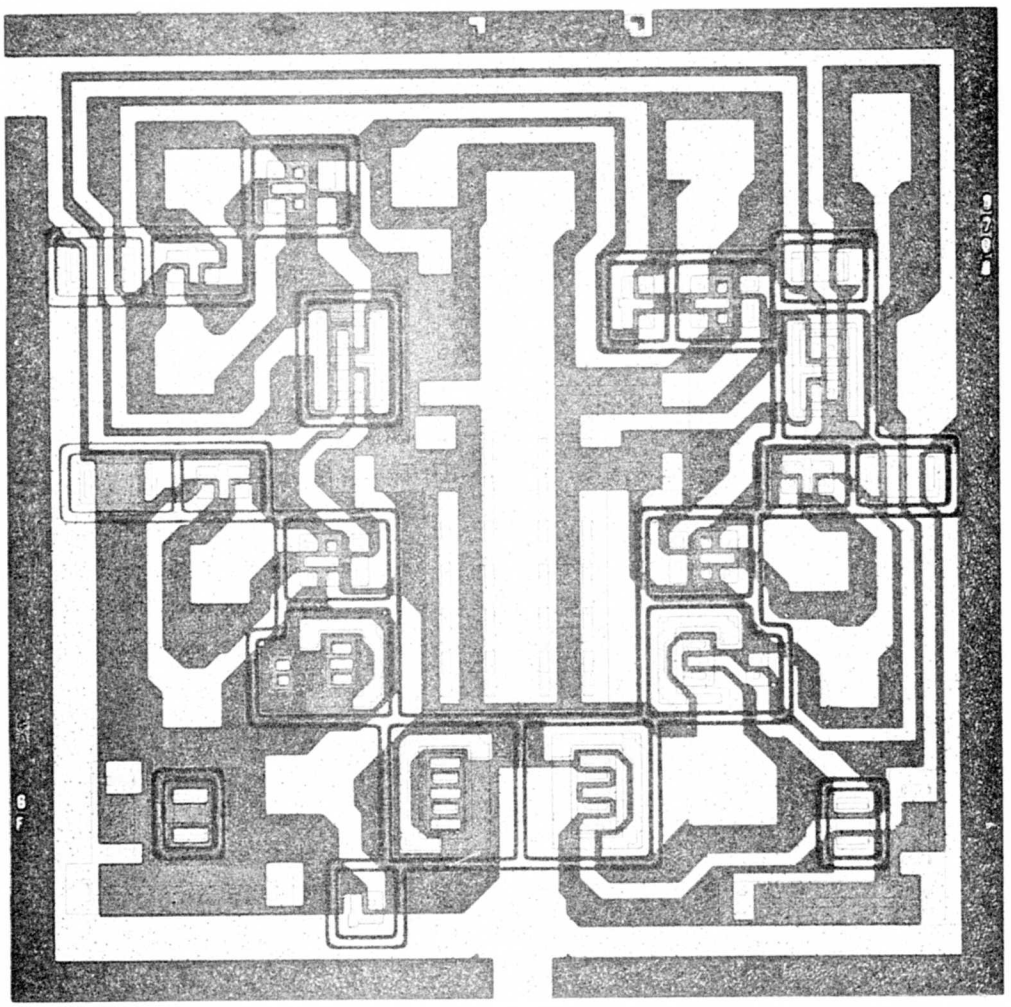


Figure 19 - An Anodized 9708 Die Having the Scribe Line Connected to the Metallization Pattern. The Connection is Made at the Upper Left Hand Corner and at the Bottom Center.

that connecting the scribe line can give great improvements where the aluminum is of substandard quality for anodization. That is aluminum deposited under undesirable conditions. In this case the difference can be between shorted and fully isolated conditions between metal lines. However, where the metal was of good quality, there was almost no noticeable difference between connecting and non-connecting the scribe lines (Figure 20). The only difference being, that the clearing at the metal line edge is better.

The conclusion then is, that scribe line connection should be used with cold substrate deposited aluminum and where the aluminum quality is marginal but it is not necessary for good aluminum.

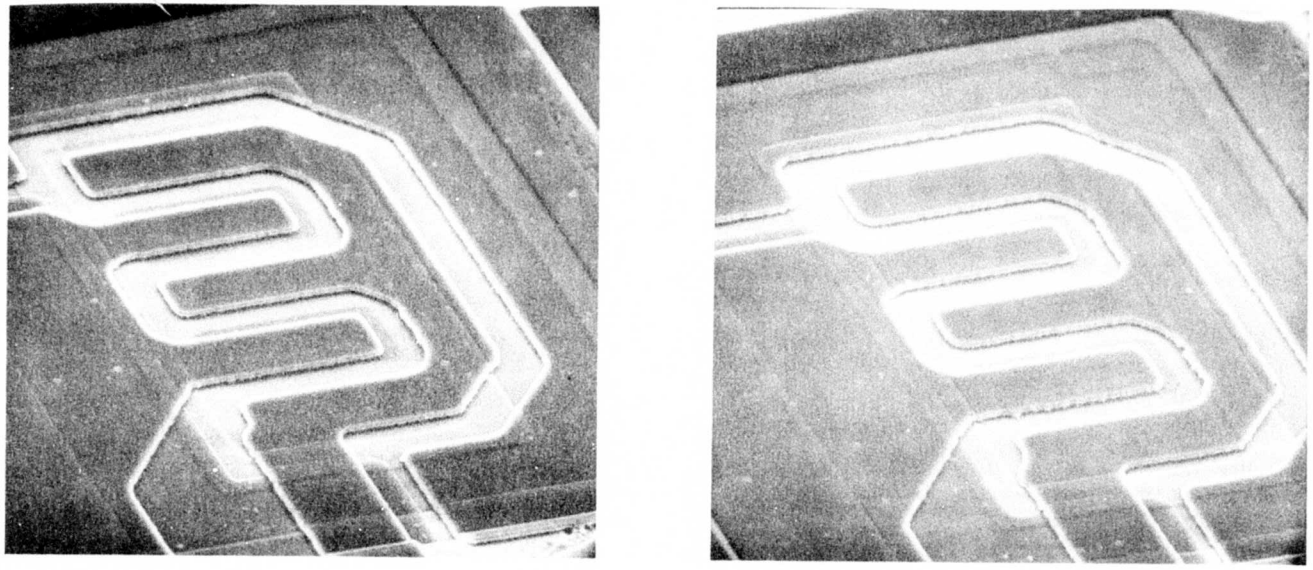
MULTILAYER METAL ANODIZATION PROCESSES

Considerations

A two level metal electrical interconnects structure consists of three parts:

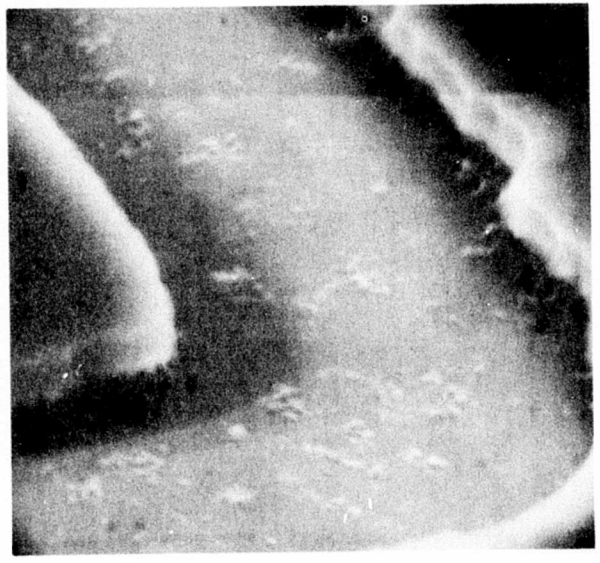
- First level metal
- Insulator
- Second level metal

First level metal processing has already been covered and the process settled upon employs a layer of vapor deposited oxide (PV_X) for the anodization mask that gives excellent yield with a high degree of control. With 2-layer metal, there may be a slight advantage in using Al_2O_3 as the masking layer for processing the first level interconnect. This is because Al_2O_3 inhibits the formation of hillocks while vapor deposited oxide (PV_X) depending on its deposition temperature,

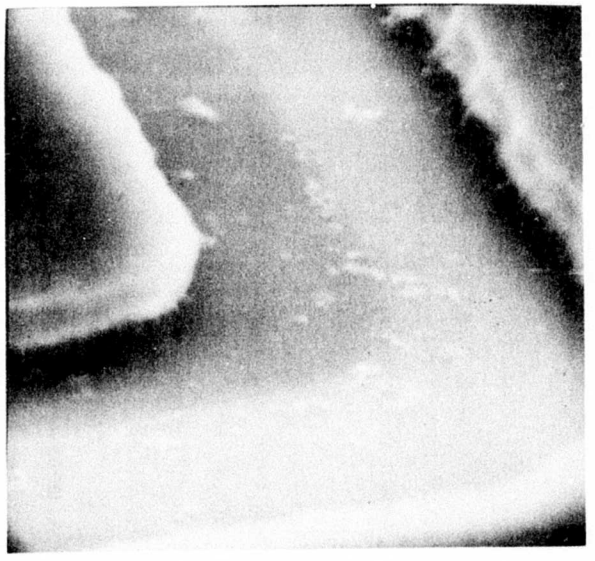


(a) (b)

Figure 20 - Scanning electron microscope comparison at 600X (a and b) and 6000X (c and d) of transistors on the same wafer after anodizing and removing Al2O3. Metal connected to scribe line during anodization (a and c). Metal not connected to scribe line during anodization (b and d).



(c)



(d)

Figure 20 (Continued)

can enhance hillock growth. Hillocks are metal outgrowths which occur on heating the aluminum and they can interfere with masking for subsequent processes. In addition to the foregoing, the thickness of the masking layer should be chosen to optimize surface profile for the subsequent processes.

The insulating layer between the two interconnect levels can consist of deposited PVx, Al_2O_3 or a combination of both. It can be formed separately, partly or all from the masking layer for first layer anodization. The dielectric constant of Al_2O_3 is about twice that of the SiO_2, thus if it is necessary to obtain equivalent capacitance between the two metal layers the thicknesses of Al2O3 must be twice that of SiO_2. The basic question is: what is the proper thickness of the insulating layer? Electrically a 3000Å layer of Al_2O_3 or PVx is far more than is necessary to isolate against the TTL circuit operating voltage. The only other consideration is interlayer capacitance and this consideration will depend on the circuit speed. In the present development, the thicknesses were kept at around 0.8, however, anywhere from 0.3 to 1μ should work satisfactorily.

In order for the second metal to make electrical contact to the first, vias are etched in the insulating layer prior to aluminum deposition for second metal. The second level metal can be processed either by anodization or by masking and etching. If anodization is used, it is necessary to at least leave the metal in the scribe line during the anodization yield. In the first layer, this function is fulfilled by leaving the scribe line open as was discussed in the previous sections.

Thus it is evident that there are a number of options in dual layer metal processing. These are: two types of masking material for first layer delineation and also for the isolation layer, and etching or anodization for the second layer metal delineation. Again the final process must be chosen on the basis of ease and reliability of manufacturing.

Test Vehicles:

Dual layer process development and prove out was carried out using the MASC test mask set and the 9780 radiation hardened integrated circuit. The test mask allows evaluation of the first metal, isolation, via resistance and second layer metal independent of each other and of device properties. This test vehicle was used to investigate and determine the relative merits of the processes to be discussed. The best process found was then proved out using the 9780 demonstration vehicle.

The vehicle originally chosen for the development of the multi-layer anodization process is the radiation hardened MSI 4-Bit shift register, the Fairchild 9780 (Figure 21). This circuit, as developed, employs: Dielectric isolation, $MoSi_2$ thin-film resistors, Dual layer aluminum metallization, and Photocurrent compensation. The 9780 circuit employs a very large die (138 mils x 98 mils) and much tighter masking tolerances than the 9702 or 9708 circuits. Because of the large die size this circuit has in past given very low yields. Although anodization will improve yield through metal processing, the major failure mode for the circuit occurs because of device failure and this will not be improved by anodization.

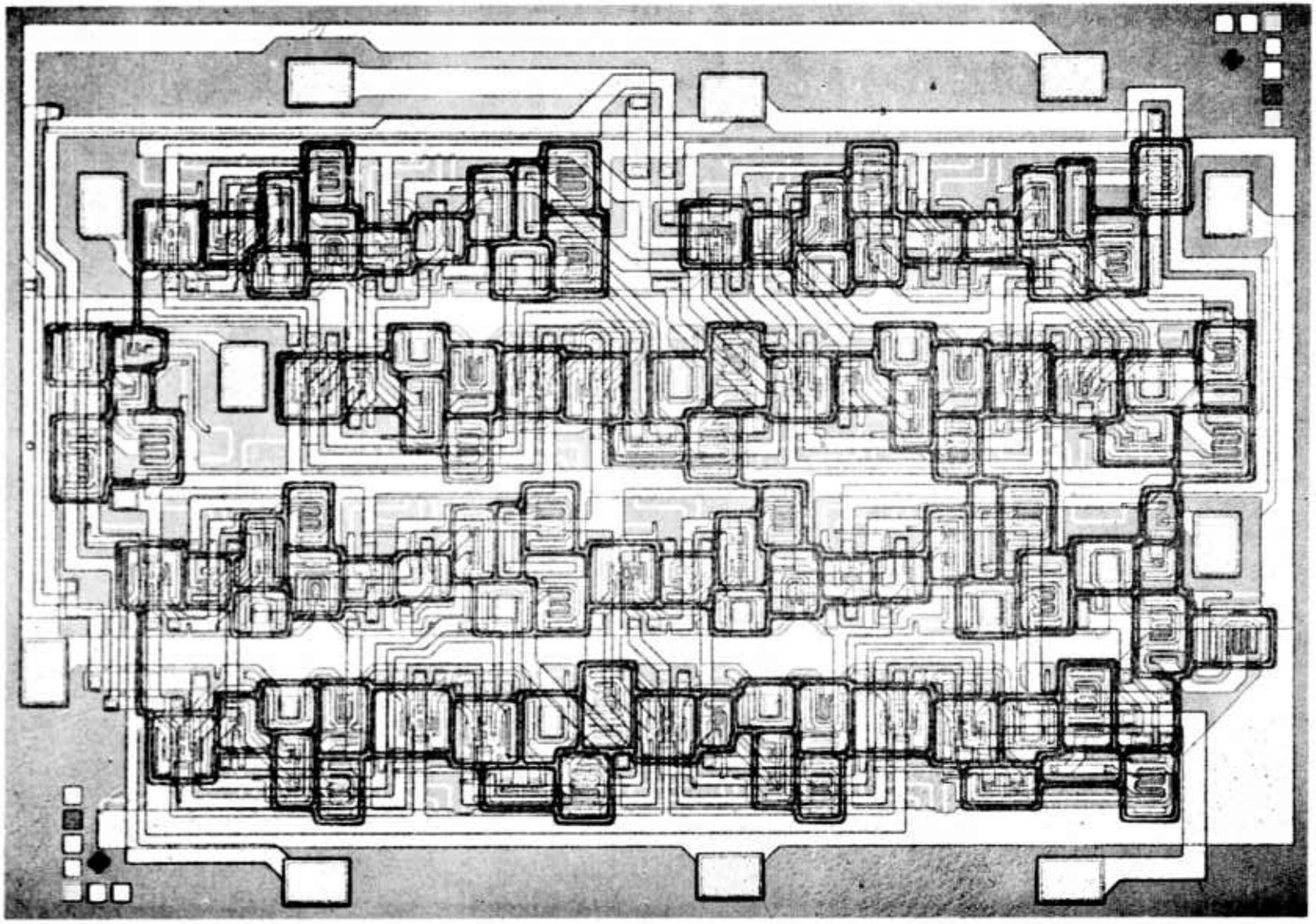


Figure 21 - A 9780 circuit, showing both metallization layers, that was fabricated using standard (non-anodized) techniques.

RESULTS

The various process options were tested and the following results obtained.

Process 1 - Anodization only Process: This process employs only aluminum anodization to achieve dual layer metal interconnections. There are two variations and these are shown in Table 2.

TABLE 2

Dual Layer Metal Interconnect Process Employing Al_2O_3 Masking:

Sequence A	Sequence B
Deposit Al (≃ 1.2μ)	Deposit a thicker Al layer (≃ 1.6μ)
Barrier Anodization (≃ 180V)	
Delineate Al_2O_3 to first metal pattern	Porous anodize 0.6μ Al (160V)
	Delineate Al_2O_3 to metal pattern
Porous anodize field (≃ 160V)	Porous anodize field (≃ 130V)
Open vias (in barrier anodization)	Open vias
Deposit Al (≃ 0.7μ)	Second metal process
Barrier Anodization	
Delineate Al_2O_3 to vias and scribe lines	
Porous anodize field	
Open vias (in barrier anodization)	
Second metal process	

Both these processes were attempted using the MASC test set. Squence A, was overwhelmingly complicated. In particular, problems were encountered in trying to sever the metal connections to the scribe lines after the second layer metal is formed, particularly if it is formed by anodization. The process is simplified if the second layer metal is defined by conventional masking and etching. Sequence B, is simpler and actually works quite well on a single wafer basis. However, for multiwafer anodization some wafers will porous anodize more rapidly than others. Therefore, the 160 volt porous anodization to produce the masking layer is hard to control. In some cases some wafers anodized almost completely while others anodized less than expected. In the multi-wafer anodization apparatus (Section IV) all wafers are electrically connected in parallel and it appears that difference in contact resistance can greatly affect the porous anodization, not that this will not affect barrier anodization which is voltage limited, nor the clearing in the porous anodization for delineation. The conclusion is that Process A is cumbersome and Process B not reliable from a manufacturing point of view.

Process 2 - PVx Masking and Insulation Process: This process employs a phosphorous doped vapor deposited oxide mask (PVx) and insulating layer between conductors. Table 3, presents two variations based on the single metal anodization process developed in this program.

TABLE 3

Dual layer Metal Interconnect Process Using PVx Masking:

Sequence A	Sequence B
Deposit Al (≃ 1.2μ)	Deposit Al (≃ 1.2μ)
Deposit PVx (≃ 0.5μ)	Deposit PVx (≃ 0.8μ)
Delineate PVx to first metal pattern	Delineate PVx to first metal pattern
Porous anodize field	Porous anodize
Deposit PVx (≃ 0.5μ)	Open vias
Open vias	Second metal process
Second metal process	

These processes were found to be simpler to carry out and more reliable than process 1. In Sequence A, the insulation layer is formed in two steps that include the masking layer and a separately deposited layer of PVx. Sequence B, does not have this separately deposited layer. While Sequence B, takes less steps, Sequence A may be more desirable for second level metal processing.

2nd Layer Metal Process: The second layer metal may be formed by anodization or by masking and etching. Either process is manufacturally feasible, however, the anodization process in this case requires more process steps without any added advantages. Therefore, etching was found to be the simplest and most manufacturable process.

Etching of the second layer metal does put some restrictions on the choice of insulating layer. The etchants used for aluminum also attack the aluminum oxide but at a much slower rate. The ratio has been found to be about 40 to 1. The etch rate of the oxide is about 15Å/second. Assuming that over-etching of the aluminum will occur for at the most 10 seconds (in the very extreme case), 150Å of oxide will be removed. This is of no consequence, but it should be realized that etching occurs not only at the top, but also on the wall of the pores. According to Sullivan and Wood,[4] the pore wall is about 70% of the barrier layer thickness or about 0.7 X 1500Å = 1050Å for our 10ma/cm^2 anodization in 4% H_3PO_4. Therefore, the final pore wall thickness would at the most be reduced to 750Å. While this thickness is more than sufficient (i.e., the integrity of the porous oxide has not been damaged), it can be seen that this etching would be another reason for using a high voltage porous anodization. On the other hand, if PVx is used for the insulating layer then it is possible to etch the second level metal without regard for the insulation layer. Thus, the use of a PVx insulating layer requires less process control.

Surface Profile: Since the major advantage of processing the first layer by anodization is improved surface profile, this section of the report is mainly concerned with the investigation of surface profile. In particular, the surface profile was studied after anodization of the first metal and after the insulation between first and second metal was completed. The anodization masking materials which were evaluated were PVx, Al_2O_3 and the Hunts G-Line photoresist.

The surface profile studies were made with a Dektak profilometer. Scanning electron microscopic examination proved fruitless because of electrostatic charging effects in the oxide. The MASC test pattern was used. The metal was deposited on oxidized wafers and then delineated by a given method. For ease of profiling, a large metal line was selected and this was usually the metal interconnecting scribe line. These results are fully representative of the situation on an actual circuit since the primary interest is the profile at the edge of a metal line. The results are shown in Figure 22 through 28.

As a starting point, Figure 22, shows the surface profile of as-deposited aluminum. The aluminum is approximately 1.2um thick and it is deposited on heated wafers (hot substrate) by electron beam evaporation. The major divisions on this graph represent 1000Å, therefore, the Dektak trace indicates a smooth surface with variations on the order of 200 to 300Å.

Figure 23 shows the surface profile obtained by the conventional technique of delineating the metallization pattern using photoresist masking and etching away the unwanted aluminum. This figure shows the metal scribe line profile after etching and removal of the resist. Note the large step (the aluminum is approximately 1.4um thick) and the smoothness of the metal surface. After deposition of a 0.6um PVx insulating layer (Figure 23b), the step remains the same, however, the surface of the line becomes rougher particularly at the sharp metal corners where nodule formation occurs. Hillock formation also contributes to the roughness. The high step and the nodule formation at the edges are the major cause of yield loss during the fabrication of the second metal interconnects. This problem is alleviated by anodization as shown in Figure 24 to 28.

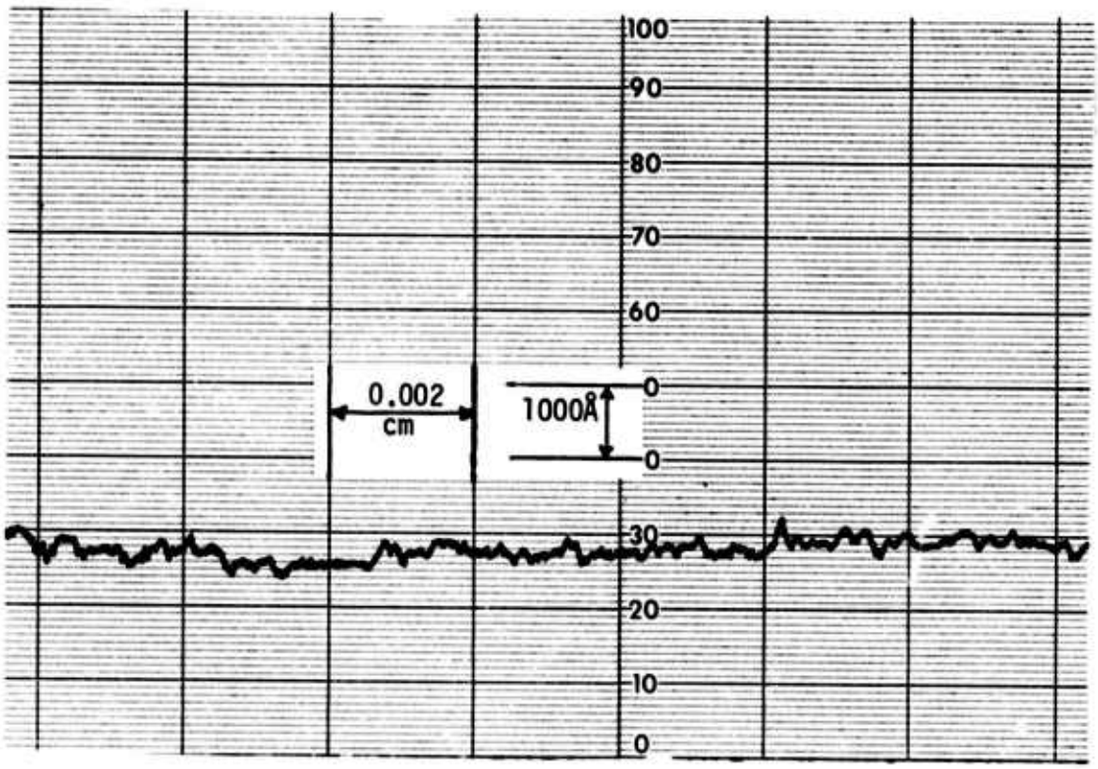
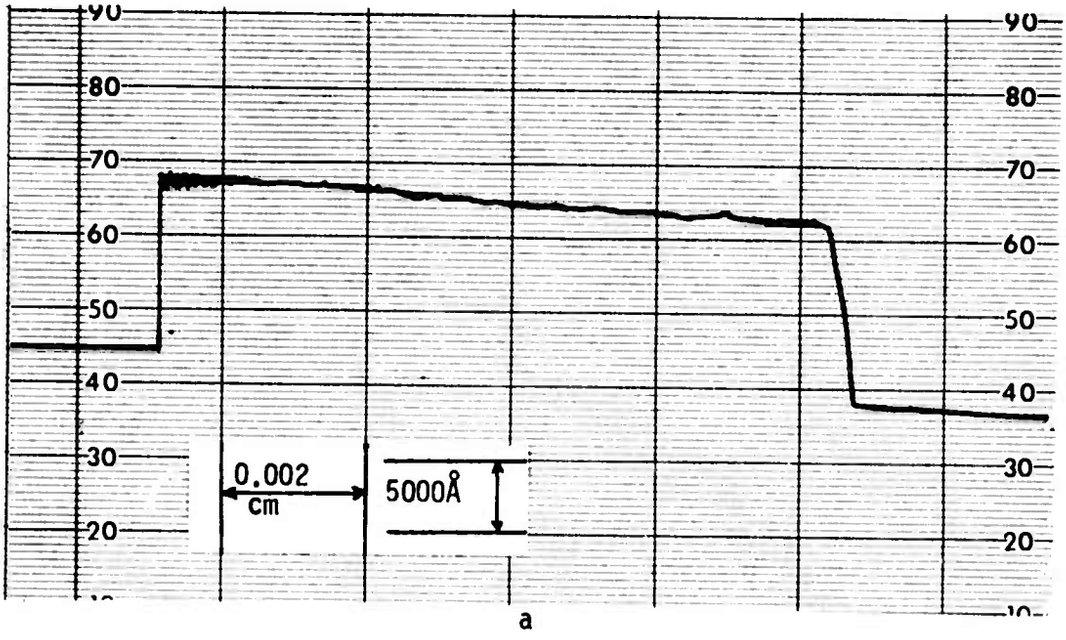
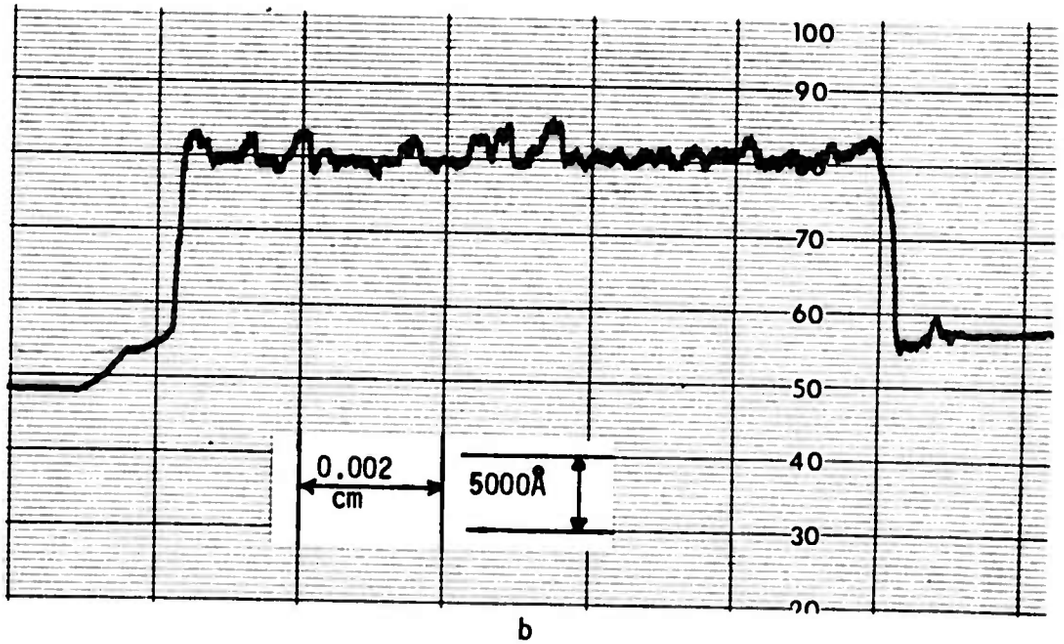


Figure 22 - Surface profile of freshly deposited hot substrate (~380°C) evaporated aluminum.



a



b

Figure 23- Surface profile on conventionally etched wafer before (a) and after PVx deposition (b).

Figure 24 shows the resulting profile before and after deposition of a 0.6μ PVx layer in the case where photoresist was used as the anodization mask for delineation of 1st layer metal. Hunts G-Line photoresist was used and the anodization was in 4% H_3PO4 at $10mA/cm^2$. Note that as expected the metal line is imbedded in the oxide and a 0.5μ step up to the porous oxide occurs because the oxide fills a greater volume than the aluminum it converts. After deposition of 0.6μ PVx (Figure 24b) the step remains the same, however, the surface roughens. Although some hillocks form in the 400^oC PVx deposition no nodules have been observed because the step (as observed by SEM[4]), possesses a more gentle contour.

Figure 25 shows the case where barrier Al2O3 formed at 180 V is used as a mask for first layer anodization. This is an especially attractive masking material because of its ability to inhibit the formation of hillocks during a subsequent PVx deposition[2]. In this process, approximately 2800Å of barrier Al_2O_3 is formed on the aluminum surface, photoresist is used to define the metallization pattern and the barrier Al_2O_3 is etched away from the area to be porous anodized. After stripping the resist the unwanted aluminum is porous anodized at 160V in 4% H_3PO_4 solution. Figure 25 shows the Dektak trace across a metal scribe line. In this case the porous Al_2O_3 is higher than the metal line and its coating of barrier Al_2O_3. This is to be expected, since the oxide fills a larger volume than the metal it converts. The step height is approximately 0.35um and remains the same after the deposition of 0.6um of PVx. Note how the barrier Al_2O_3 inhibited the formation of hillocks (Figure 25b).

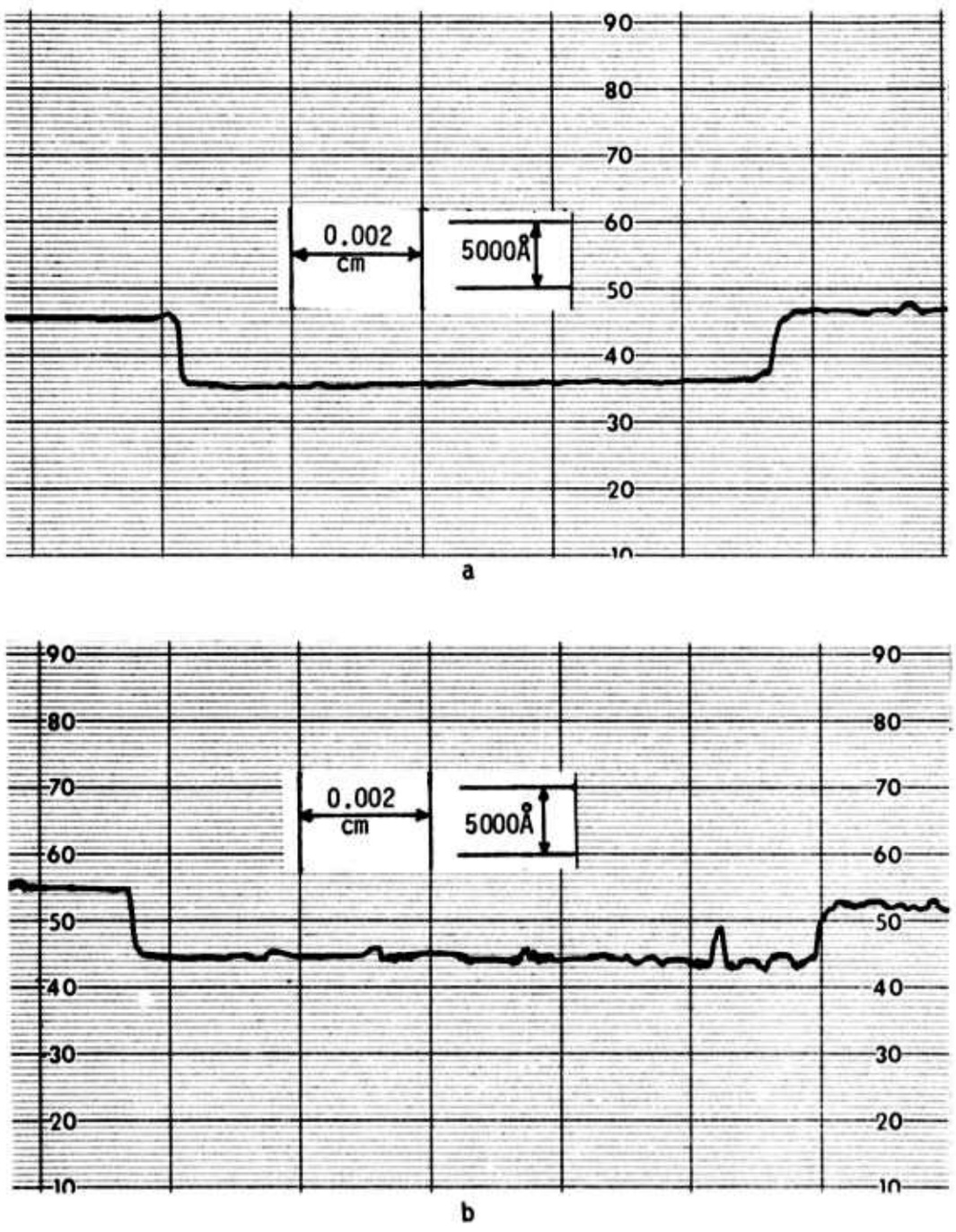


Figure 24 - Surface Profile of anodized line in the case where photoresist was used as the anodization mask, before (a) and after PVx deposition (b).

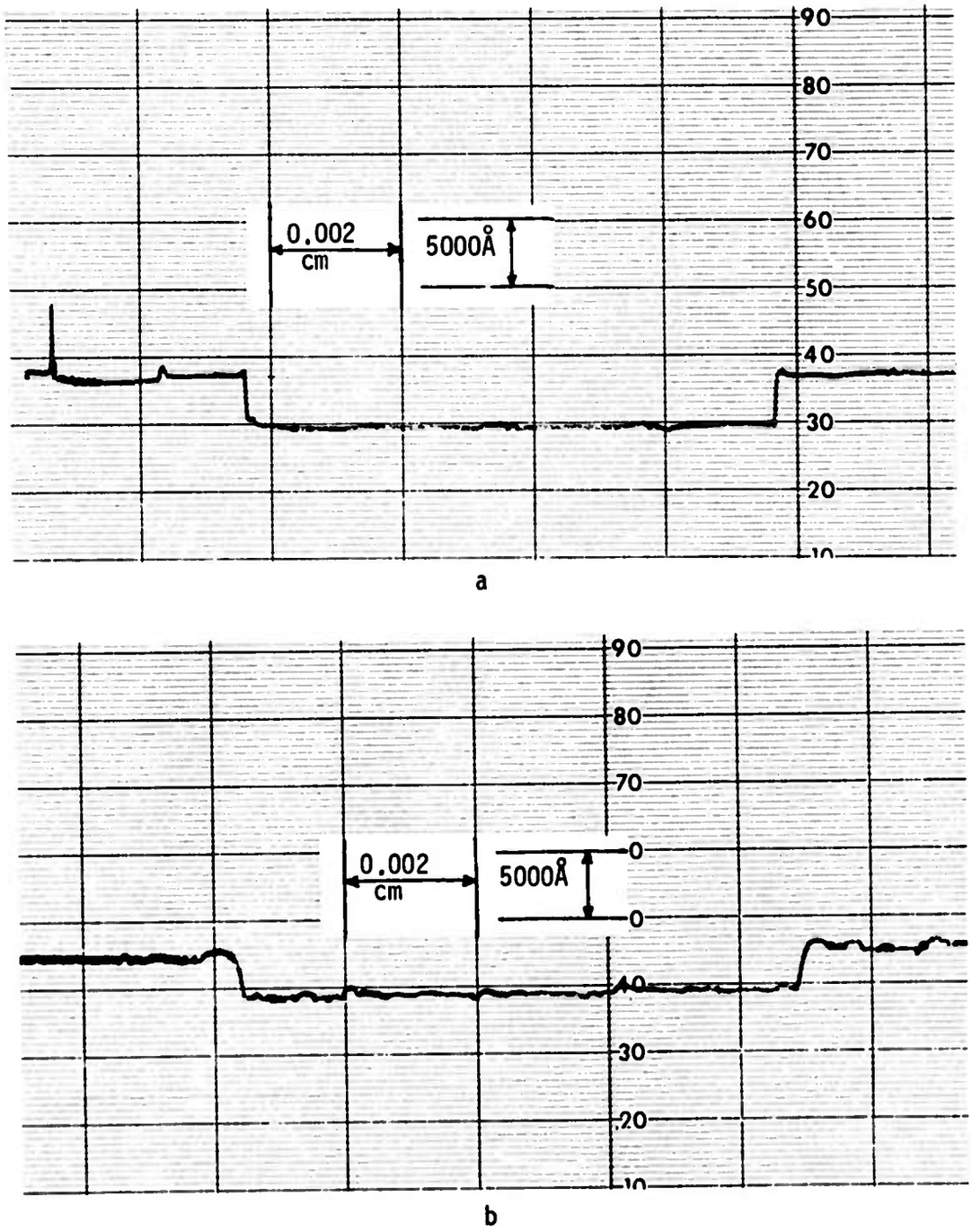
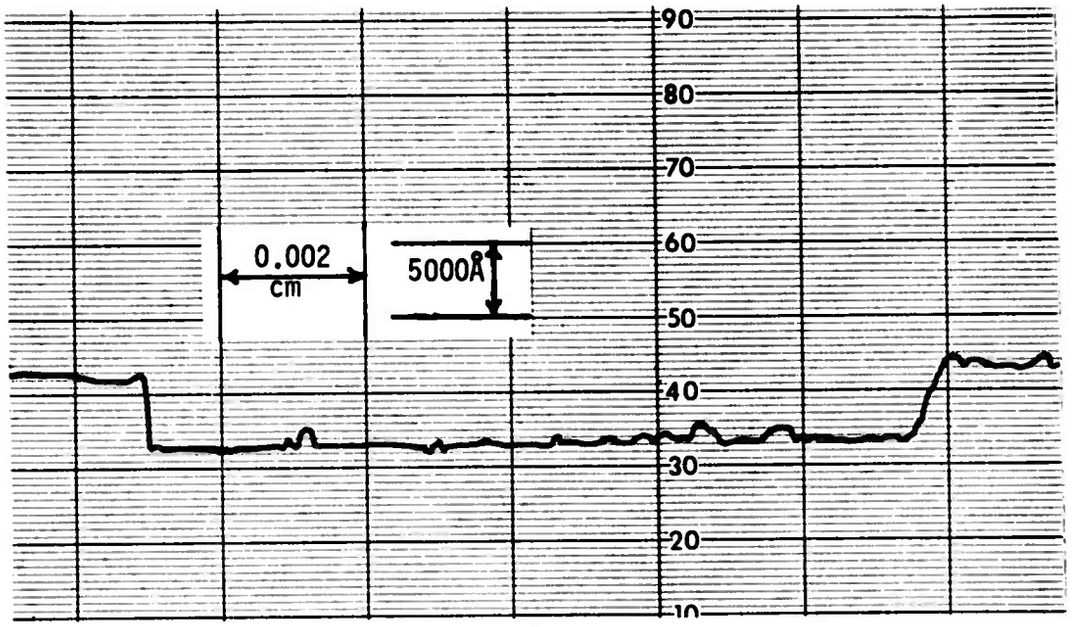


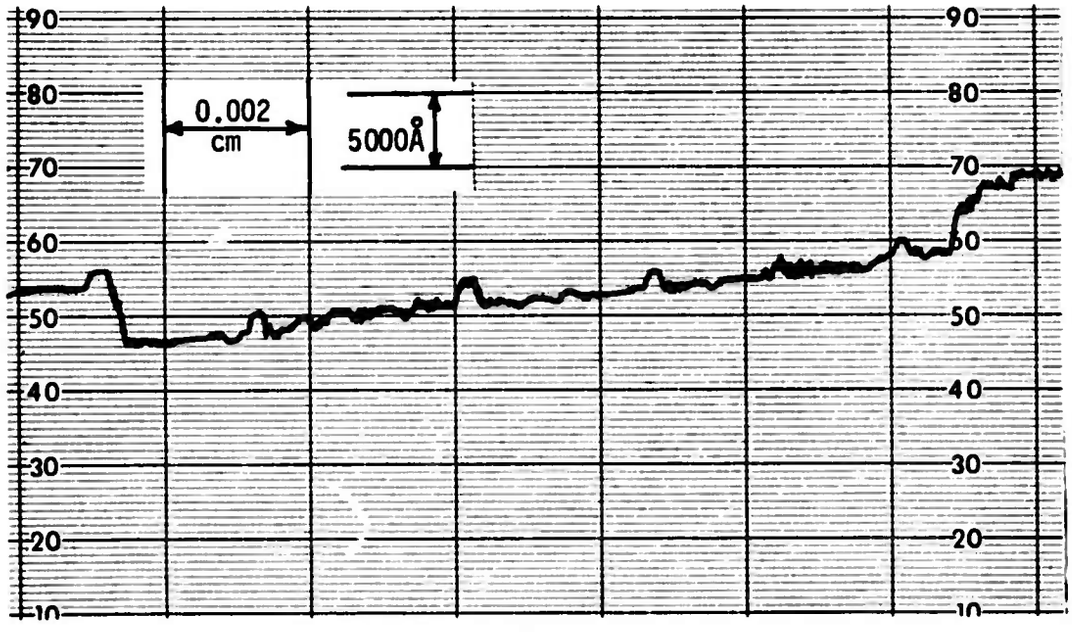
Figure 25 - Surface profile of anodized metal using a 180 volt barrier layer Al2O3 anodization mask, before (a) and after PVx deposition (b).

A variation of the foregoing process uses barrier Al_2O_3 formed at 180V as the anodization mask, but in this case, the aluminum areas to be porous anodized were protected by photoresist during the barrier anodization, thereby eliminating the Al_2O_3 etching step. That is, the inverse metallization pattern is first defined on the aluminum surface with photoresist, i.e., no photoresist in the desired metallization pattern. Next the metallization pattern is barrier anodized at 180V, the photoresist is removed and the unwanted aluminum is porous anodized at 160V in 4% H_3PO_4, Figure 26 shows the results. Again the porous Al_2O_3 is higher than the barrier Al_2O_3 covered scribe line. In this case the step height is approximately 0.5μm. The difference in step height between this and the previous process is due to the fact that in the former process the barrier Al_2O_3 is etched from the areas to be porous anodized and reduces the aluminum thickness in this area by approximately 0.2μm. Since no aluminum was removed from the areas to be porous anodized in this process an increase in step height is to be expected if the original aluminum thickness was the same for both processes. The high surface roughness evident in Figure 26b on the aluminum scribe line is probably due to a rough PVx deposition which occasionally occurs.

Turning to PVx anodization masking material, Figure 27 shows the profile obtained in the single level aluminum anodization process developed in this program. Approximately 0.6μ PVx was used as the anodization mask in this case. Note that the PVx covered metal line is higher than the porous Al_2O_3. The resulting step is about 0.2 to 0.3μ high. The surface profile obtained by this process (essentially Sequence A, Table 3) is shown in the SEM micrograph given in Figure 20 from a 9708 circuit processed in this manner. Although some hillocks are present because of the PVx deposition, the surface profile is very conducive to 2nd layer metal processes.

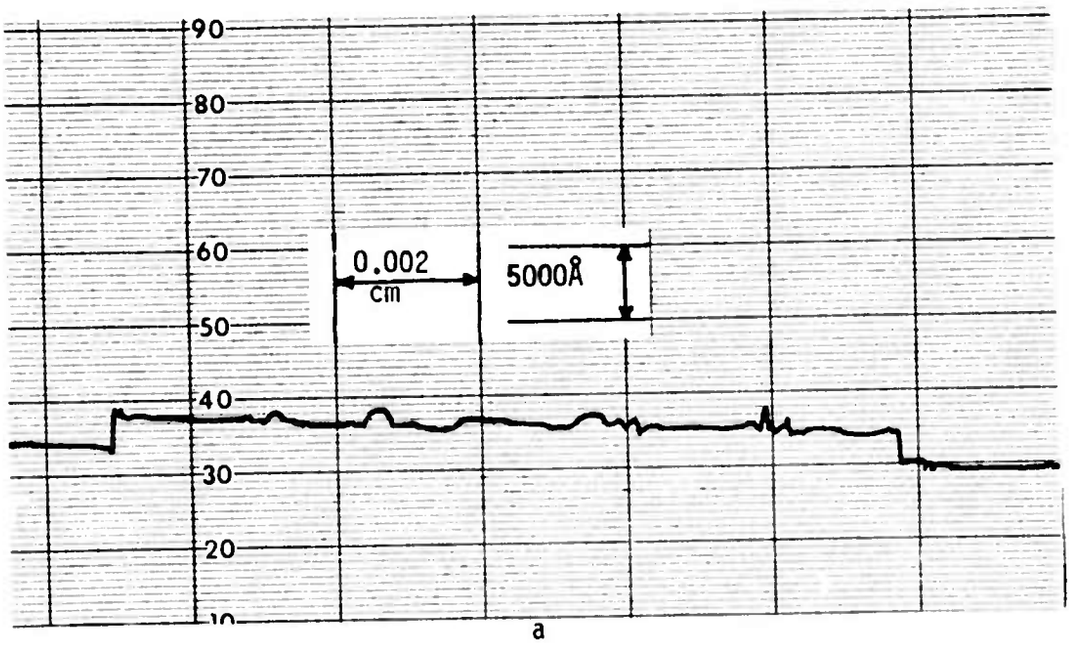


a

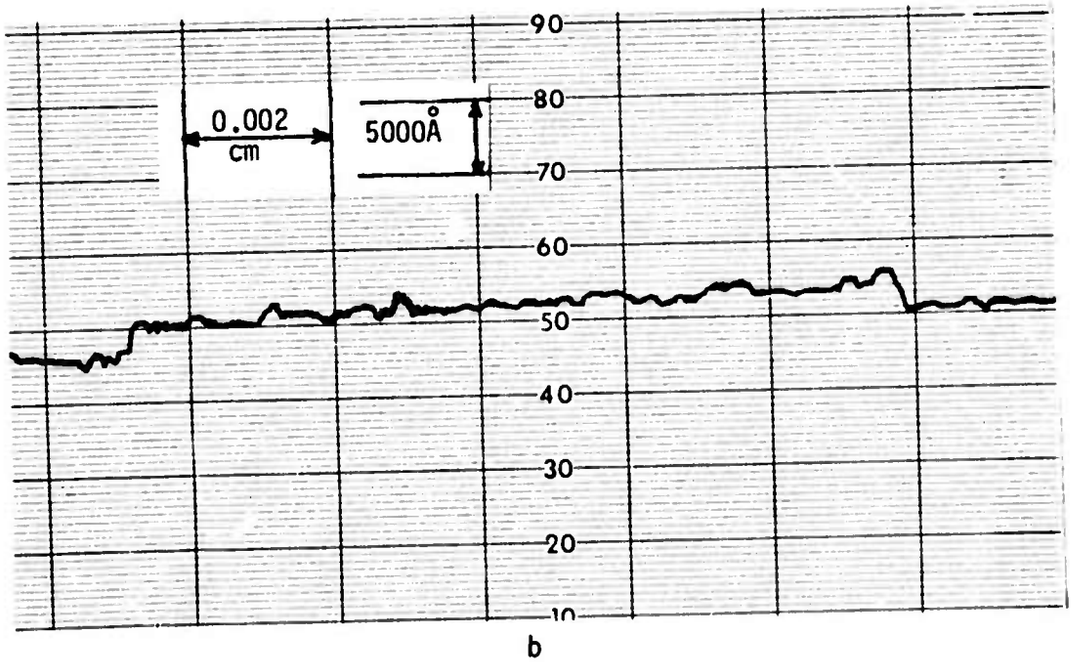


b

Figure-26 - Surface Profile of anodized metal before (a) and after PVx deposition (b). Anodization mask is barrier Al_2O_3 formed to the metal pattern by protecting the rest of the area with photoresist.



a



b

Figure 27 - Surface Profile for Metal line fabricated by the standard single layer anodization process, before (a) and after the 2nd PVx deposition (b).

It is apparent that by proper choice of the thickness of the first PVx layer, the step can be eliminated. However, this requires good control of the PVx and aluminum thickness. Figure 28 shows a case where this was done and except for the hillocks the step height appears to be 500Å to 1000Å. In fact, it is only the presence of the hillocks that indicates the location of the metal line. Thus, it is possible to achieve a flat surface profile with anodization.

Finally, it should be mentioned that it is also possible to obtain a flat surface profile when porous Al_2O_3 is used as the anodization mask as in sequence b, Table 2.

Final Two Layer Metal Process: The final two layer metal process arrived at in the present program is outlined in Table 4.

TABLE 4

An outline of the anodization process for multilayer circuits

Deposit Al (1.2μm)
Barrier anodize to inhibit hillock growth (optional)
Controlled PVx deposition (0.3μm - 0.5μm)
Delineate PVx to metal pattern
Delineate barrier Al_2O_3 to metal pattern (optional)
Porous anodize (160V)
Deposit PVx insulation (0.5μ)

Mask and etch vias to 1st level metal
Deposit 2nd layer metal (≃ 1μ)
Mask and etch second level metal
Deposit protective PVx layer
Mask and etch bonding pads
Aluminum alloy

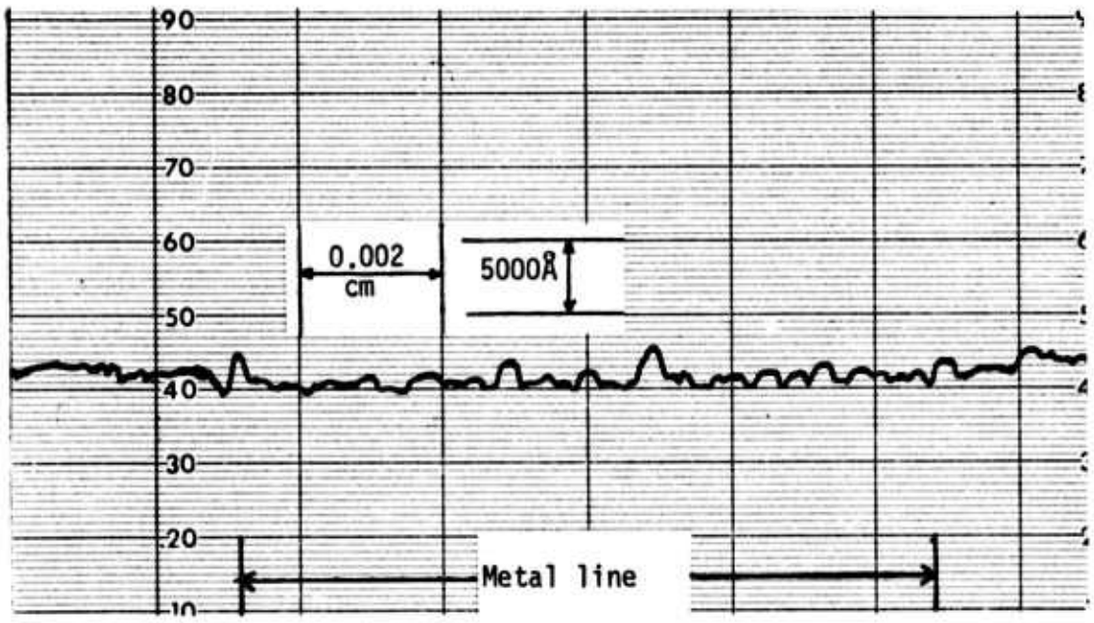


Figure 28 - Optimum Surface Profile realized using approximately 4500Å PVx anodization mask.

This process combines the single layer anodization process with a PVx insulating layer and conventional etching of the second layer aluminum. This process is capable of producing a flat surface through proper choice and good control of Al and PVx thicknesses. Even with the present manufacturing tolerances, step heights of less than 0.3μm are reproducibly achie This step height does not present any problems in second layer metal processing. A barrier anodization is included in order to inhibit hillock formation. This anodization need only produce about 1000Å of Al_2O_3 since this is sufficient for the purpose outlined [2]. In the present work an 80 volt barrier anodization in 4% citric acid was used. Although our observations did verify that hillock growth was in fact inhibited, our data is not sufficiently clear cut in favor of this extra step. This data can only be obtained by processing a large number of circuits on a regular basis. This could not be done within the scope of this program. If barrier anodization is included then it is also necessary to etch this film from the areas to be porous anodized. This can be done directly after the PVx is etched in which case the PVx layer acts as the mask for etching Al_2O_3. This procedure must also be repeated when etching the vias. The final PVx layer is a protective layer and the bonding pads are the areas to which external connection to the circuit is made.

Figures 29 and 30 show various stages of two level metal fabrication for the 9780 circuit. The photos are taken of the 9780 test pattern circuit because it is easier to discern first and second level metal, and resistors. The two layer metal was processed according to the process in Table 4 with the optional steps left out. Figure 29 (a) shows the circuit after completion of first metal, insulating (PVx) layer and vias. Figure 29 (b) shows the same area after completion of the two level metal process. The two levels of metal can be distinguished by noting that the 2nd level is more reflecting than the first. Note also, that the thin film resistors are visible even though there are various dielectric layers

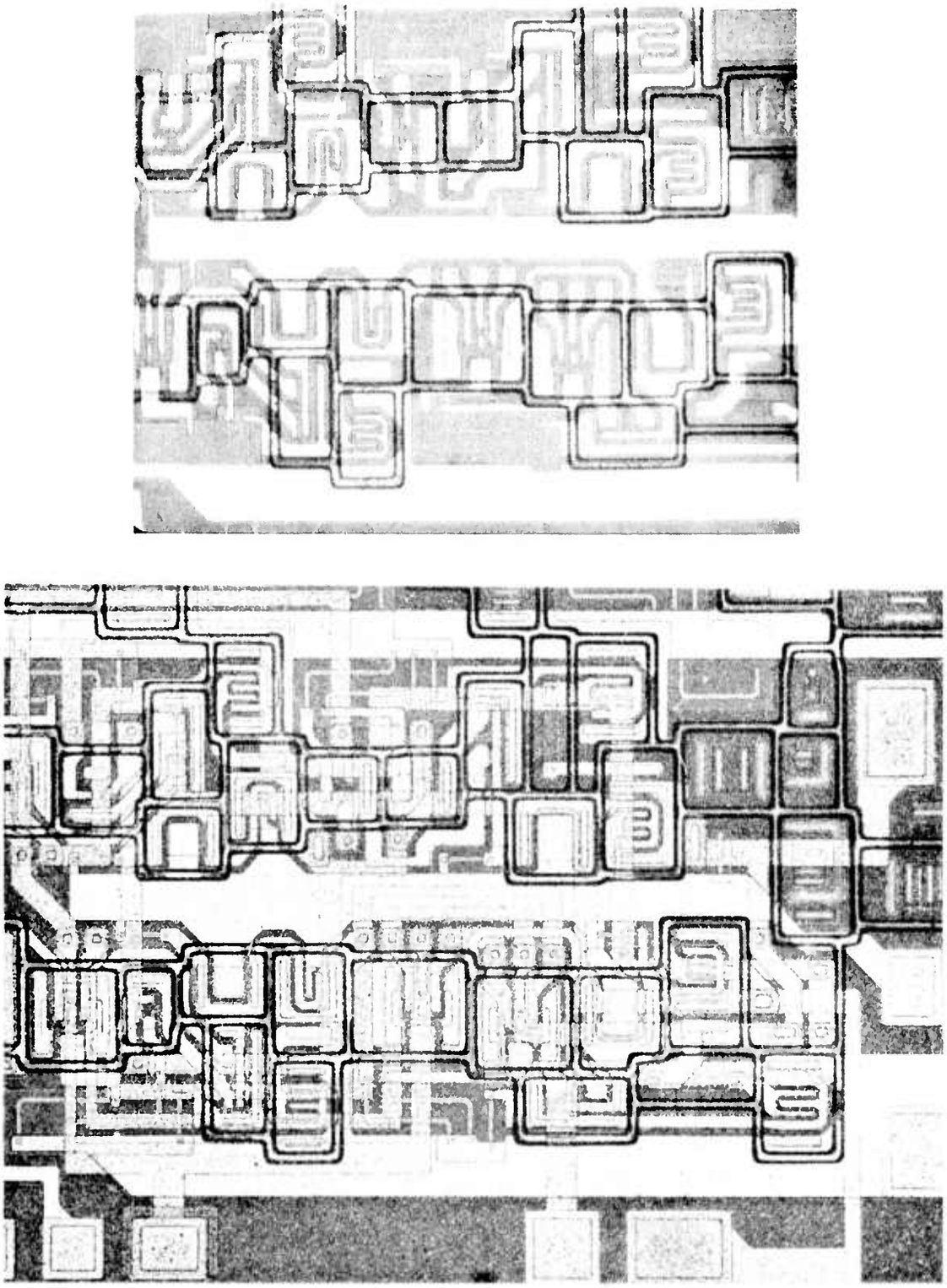


Figure 29 - A portion of the 9780 circuit after various steps in two layer metal fabrication (a) After anodization of 1st metal, insulator deposition and formation of vias (upper photo) (b) Two layer metal process completed (lower photo).

covering them. Starting at the resistor surface, these dielectrics are 0.3µm SiO, 1.6 µm Al_2O_3, and 0.8 µm PVx. Figure 30 is a scanning electron microscope micrograph showing the surface profile just after defining the second layer metal. A very desirable surface topography is realized with the process in Table 4.

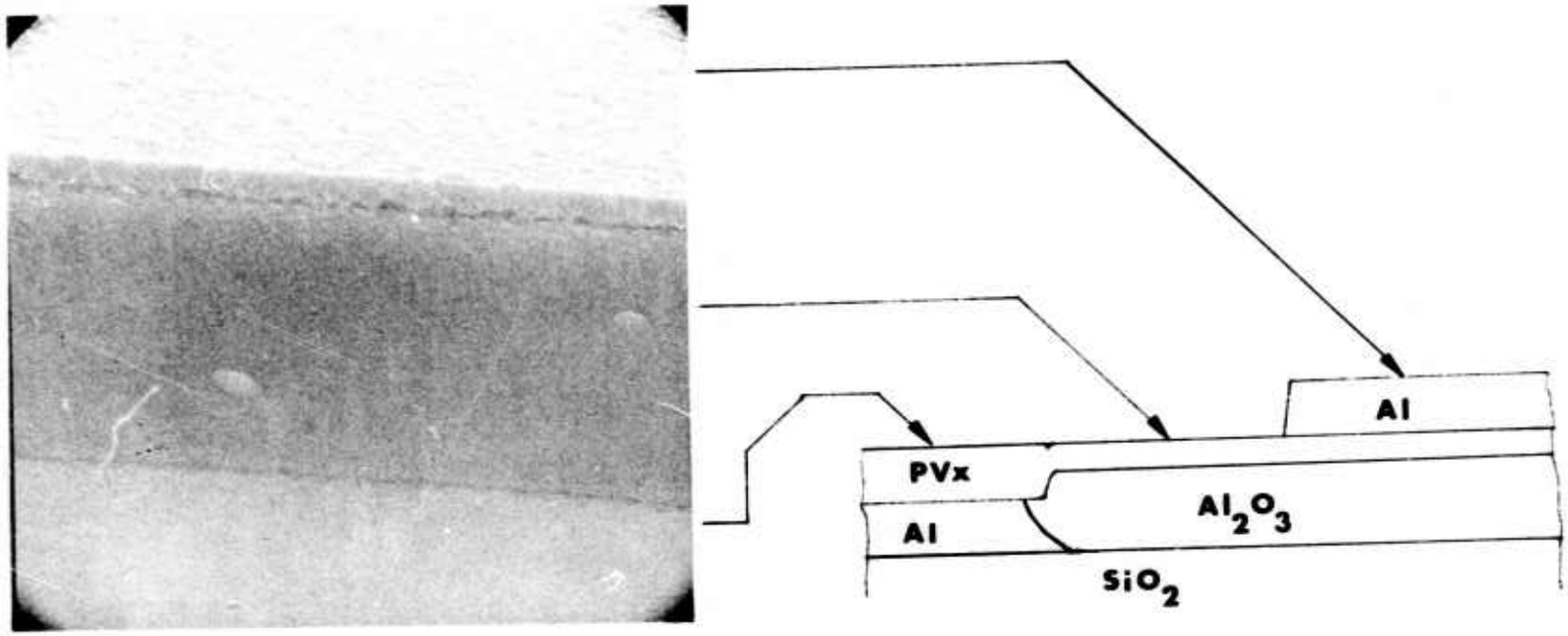


Figure 30 - Scanning electron microscope micrograph at 2000X of surface after delineating 2nd layer metal on a 9780 circuit. Drawing to the right, explains the observed features in cross-section.

SECTION III
THIN FILM RESISTOR PROCESS

INTRODUCTION

One of the basic requirements placed on a new process is that it be compatible with existing processes. Alternatively, if this is not the case, existing processes should be easily modifiable to achieve compatability. In this section it is shown that the aluminum anodization results in electrochemical attack to the underlying resistor. Since all thin film resistor materials are more or less subject to electrochemical attack, the solution to this incompatability is to protect, or passivate, the resistor with an insulating film. The question of compatability is now transferred from that of anodization to that of the resistor protection process. Fortunately, a wide variety of passivation materials and processes are available and several were found to be compatible. Silicon Nitride was the first dielectric chosen for resistor passivation. Although this material met all of the passivation requirements, it proved to be unsatisfactory mainly because equipment limitations on temperature control affected the reproducibility of the thin film resistor values. Silicon monoxide was substituted for Si_3N_4 and proved to be satisfactory. This section of the report describes the problems encountered with Si_3N_4 and their solution, the silicon monoxide passivation application and the final passivation process in detail.

THIN FILM RESISTOR PROPERTIES AND FABRICATION

The radiation resistant circuits used in this program utilized 200Ω/molybdenum disilicide ($MoSi_2$) thin film resistors developed by Fairchild. $MoSi_2$ is a direct replacement for NiCr thin film resistor material and has the following advantages: 1) easier processing, 2) compatible with high temperature dielectric deposition process, 3) self passivating and 4) higher specific resistance and therefore,

greater thickness for the same resistance leading to improved reliability. The properties of MoSi are given in Table 5.*

TABLE 5

Nominal $MoSi_2$ Resistor Characteristics

Sheet Resistance (Ω/sq)	200
Film Thickness (A)	600-900
Film Resistivity ($\mu\Omega$-cm)	1400
Temperature Coefficient of Resistance (50 - 150°C) (ppm/°C)	-150
Composition	63 Wt. % Mo.
Reproducibility (for 0.4 mil line width)	± 20%

The $MoSi_2$ films are deposited by d-c diode sputtering in a fully automatic magazine-fed sputtering machine. Each wafer is brought under the sputtering cathode and deposition is carried out for a specified time under carefully controlled conditions. A high degree of uniformity is maintained across a wafer and from wafer to wafer within a run.

After deposition, the $MoSi_2$ resistors are delineated either by a lift process or by masking and etching. In lifting, a prepatterned underlying film is dissolved away, thereby removing the unwanted overlying resistor material.

* A review of properties and reliability of MoSi2 resistors appears in the 1st Interim Report for this program.

METHODS OF INVESTIGATION

Investigations required for assessing the manufacturing compatibility of the resistor and anodization processes was most easily obtained using a resistor test pattern and later verified on actual circuit wafers. This mask set, designated as XRA, was designed for testing thin-film resistors. The mask set incorporates the option of passivating the resistors which of course would be necessary if the anodization processes affect the resistors. A photograph of the XRA test pattern is shown in Figure 31. The resistors are 1, 5, 10, 25 and 50 squares in length.

One of the methods used extensively in this work is to design investigations such that, where possible, the desired comparison (of process change, treatment etc.), is obtained from different portions of the same wafer. This type of comparison eliminates wafer to wafer variations and ensures, except at the process where the comparison is to occur, that the comparison is made from regions processed in exactly the same manner. Of course, variations across a wafer must still be taken into account. For example, resistor values may vary $\pm$ 10% from wafer to wafer; however, across a wafer the variation will be less and hence the comparison more conclusive.

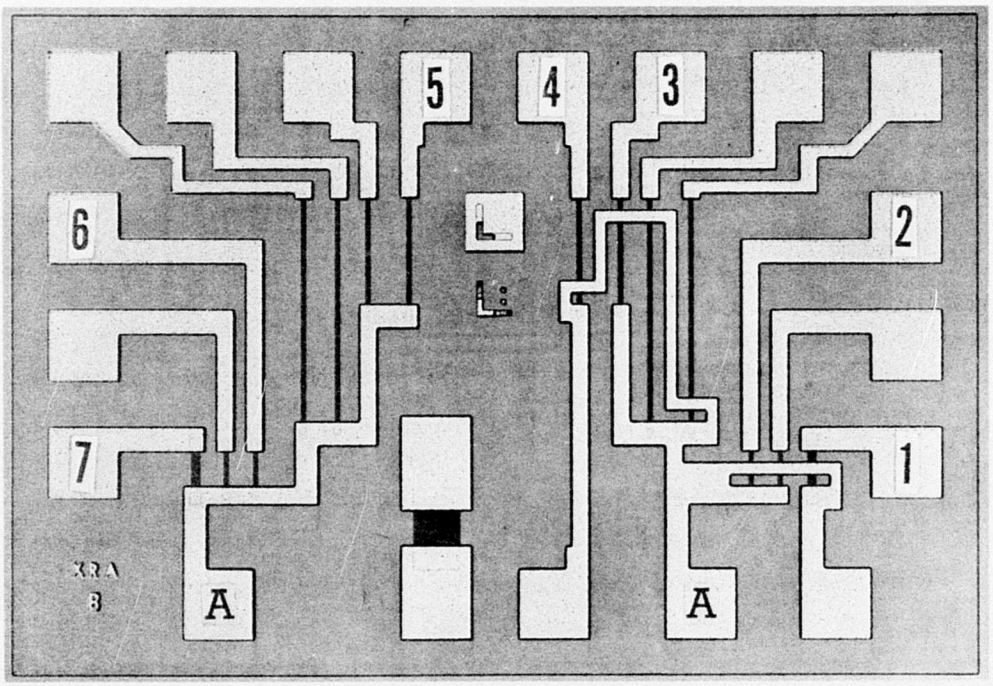


Figure 31 - XRA Resistor Test Array

EFFECTS OF ANODIZATION ON THIN-FILM RESISTORS

Since aluminum delineation by anodization requires complete anodization of the aluminum above the resistor two possible effects on thin film resistors could occur. First, the aluminum particles ("snow") left after anodization may form a conductive path and decrease the resistor value, and secondly, the resistor itself may be anodized increasing its resistance. In either case, protection of the resistor material would be necessary.

The effects of anodization were determined as follows: First, the anodizability of the thin-film resistor material was determined and secondly, resistor test patterns and integrated circuits with thin-film resistors were processed through metal anodization. Although the resistor material to be used on this program is $MoSi_2$, the effects of anodization on CrSi resistors was also studied because CrSi is a thin-film resistor material which is also used in low-power radiation-hardened integrated circuits. However, since the results for CrSi were essentially the same as for $MoSi_2$ only the latter results will be presented.

To begin these studies, $MoSi_2$ films, 1500 Å in thickness, were deposited on oxidized silicon substrates. The films were subjected to various anodization solutions, i.e., the three percent tartaric acid, the four percent H_2SO_4, and the four percent H_3PO_4. The quality of the $MoSi_2$ surface was determined prior to and after the treatments by ellipsometry. (Ellipsometry is an optical technique which is very sensitive to surface properties. It can be used to detect changes in the properties or the thickness of very thin layers).

With no applied voltage to the film, no change in surface quality was measured after exposure of $MoSi_2$ to the three solutions for times exceeding a half hour. With positive voltage applied, appreciable anodic currents would flow at voltages well below those normally used in aluminum anodization. For example, in four percent H_3PO_4 at 10 volts, the current started at 25 mA and then decayed to zero in one to two minutes. At five volts the current was less, starting at about 2 mA and decreasing almost linearly to zero in less than one hour. Similar results were observed when using the other solutions. Anodization did occur at these low voltages as was evidenced by interference colors (blues, golds, yellow, etc.). The 1500 Å $MoSi_2$, film as deposited, normally appears metallic gray. As expected, the interference colors were less uniform for the high than the low applied voltage. This is because the material is a resistor and therefore anodizes more rapidly close to the point where electrical contact is made. Electrical measurements indicated that the anodization had turned the resistor to a fairly good insulator. These results indicate that although $MoSi_2$ is stable in these electrolytes with no voltage applied, it may be easily anodized in the same electrolytes.

For the aluminum anodization studies, resistors were prepared in the following manner. The resistor material was deposited on oxidized silicon wafers, resistors were delineated, aluminum deposited, and the metal pattern protected by vapor deposited SiO_2. For direct comparison, part of the aluminum on the wafer was delineated by standard etching techniques while the remainder was delineated by anodization. Again several anodization current densities and two solutions were used.

When the aluminum was delineated in four percent H_2SO_4, the resistor values increased, and in many cases appeared open (resistance greater than 15 megohms). When the aluminum was delineated in four percent H_3PO_4, both increased and decreased resistor values were observed. The effects of anodization were less pronounced in four percent H_3PO_4, and in most cases were within ±25 percent of the original value. A small sample of the data is given in Table 31.
through 7 of test array in Figure

TABLE 6

Anodization Effects on Unpassivated Resistors

WAFER NO. 1 (Resistance in Kilohms)							
Anodized	R1	R2	R3	R4	R5	R6	R7
No	5.912	5.701	11.890	11.653	2.438	2.428	1.288
No	5.776	5.888	11.826	11.594	2.337	2.324	1.274
Yes	5.235	5.109	10.790	10.600	2.100	2.090	1.112
Yes	5.053	5.044	10.240	10.500	2.081	2.020	1.120
Yes	5.242	5.400	10.940	10.77	2.046	2.025	1.150
WAFER NO. 2 (Resistance in Kilohms)							
No	4.850	4.850	9.770	9.880	2.001	1.992	1.093
No	4.930	4.920	9.870	9.880	2.001	1.989	1.078
Yes	5.515	5.318	11.139	11.092	2.189	1.107	1.236
Yes	4.950	4.850	10.640	11.160	1.680	2.047	1.206
Yes	8.435	10.110	15.480	0.707	0.682	0.668	0.670

Evidence of anodization was also observed optically and by scanning electron microscopy. Figures 32 and 33 show the effect of anodization on unprotected resistors on 9702 and 9708 wafers .

It is apparent from the foregoing data that resistor passivation against anodization is necessary. The passivation must be a non-conducting layer deposited after resistor fabrication. The layer must be compatible with the resistors and must be selectively removable from the resistor ends to facilitate electrical contact to the resistors. There are a number of dielectric materials suitable for this purpose. For example, evaporated SiO, sputtered quartz and Si_3N_4. The initial choice was Si_3N_4 because of its good insulating properties and because it may be selectively etched from over the resistor. SiO and quartz must be removed by lifting which, perhaps, is not as desirable as etching but has been used for many years in the fabrication of radiation hardened circuits. Vapor deposited oxides are less desirable because, they must be removed by etching and the available etch solutions attack the underlying resistors as well as the highly soluble phosphorous glass formed in the emitter process.

SILICON NITRIDE PASSIVATION

9702 and 9708 wafers were processed using Si_3N_4 passivation. Several problems arose: Targeting of resistors, difficulty in etching Si_3N_4 and there were also some equipment related problems. The processing, tests and results are described below:

Process: The silicon nitride deposition is carried out in an Applied Materials Nitrox TM infrared-heated reactor. The deposition employs the thermally induced reaction of silane and ammonia in a nitrogen ambient. The deposition temperature as recorded by an optical pyrometer is 770°C (not corrected for emissivity). The thickness of silicon nitride is nominally 1000Å. The optical and etch characteristics of the Si_3N_4 were monitored to ensure Si_3N_4 of proper quality.

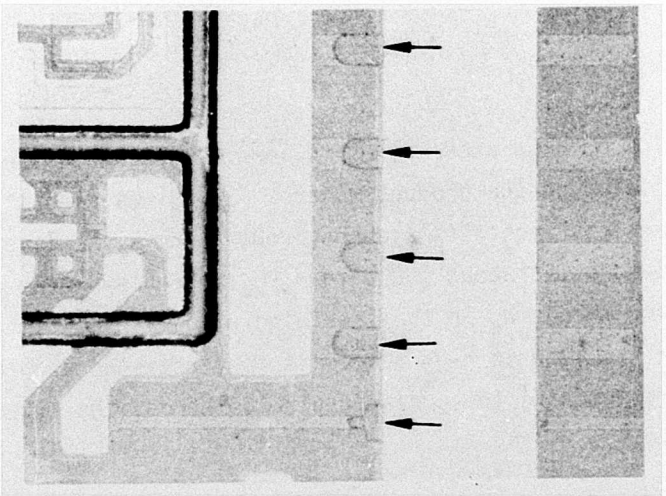


Figure 32 - Part of an Anodized 9708 Die. Arrows point to Partially Anodized Resistors.

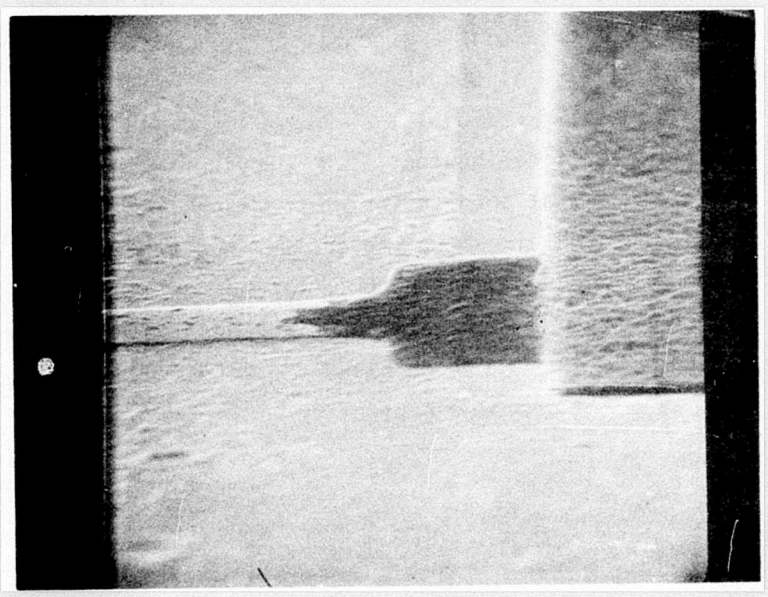


Figure 33 - SEM Photograph Showing Partially Anodized Resistor (Dark Area) after the Porous Al_2O_3 Was Removed

The process used was as follows: Resistors were deposited and delineated on the product wafers. Si_3N_4 was deposited and the device and resistor contacts etched through the Si_3N_4 layer. Etching was carried out at about 150°C in H_3PO_4. Problems were encountered with etching the Si_3N_4 in that staining of device contact areas occurred which resulted in high device contact resistance. This was overcome by etching the contact cuts to the devices after the Si_3N_4 was etched.

Anodization Resistance of Si_3N_4: A direct test of the anodization resistance of Si_3N_4 was not made because previous work to determine the effects of anodization on Si_3N_4 has shown that this thickness (1000Å) is more than sufficient to prevent anodization of the resistors. For example, it will take more than half an hour at 300 volts to convert 1000Å of Si_3N_4 to anodic oxide [5]. For the voltages and times required for aluminum anodization very little, if any, anodization of Si_3N_4 will occur.

However, verification that Si_3N_4 provides excellent protection to resistors against anodization was made on XRA test structures and on 9708 integrated circuits. Again the investigation was conducted such that a direct comparison could be made on each wafer between passivated resistors with metal anodized and those with metal defined by etching. No effect was observed and it was concluded that Si_3N_4 provides adequate resistor protection.

Resistor Targeting: As anticipated, the high temperature Si_3N_4 deposition process affected the thin film resistors and also resulted in large variation of resistance values from wafer to wafer. Tests were made which compared a portion of a passivated resistor wafer with a portion of the wafer removed prior to passivation. The results indicate a decrease in film resistivity of 50% which was adjusted for by a similar decrease in film thickness. Figure 34 shows the relation between resistor deposition time (sputtering time) and sheet conductance for nitride-passivated resistors. Also shown is the same relation for the standard $MoSi_2$ resistor process (no passivation). From this curve a target deposition time of ≈100 seconds gave 200Ω/□, 630 Å $MoSi_2$ resistors.

The variation in resistance values was found to be due to variations in temperature from wafer to wafer during the Si3N4 deposition. As much as a 50°C difference was measured on our engineering reactor. That this can have a significant effect is demonstrated in Figure 35 which shows the resulting sheet resistivity at various Si3N4 deposition temperatures for resistors which would nominally be 200Ω/□ if no passivation were used. It can be seen that the sheet resistance changes by as much as 30% from 750 to 850°C deposition temperature. The difference between the R&D and the Engineering reactors is due to a different method of temperature measurement. The former uses a thermocouple inbedded in the susceptor while in the latter the temperature is assessed optically.

Investigations were also carried out to determine if a reaction between Si_3N_4 and $MoSi_2$ occurred during the deposition. Comparisons were made between resistors covered and not covered with SiO and then subjected to Si_3N_4. No difference in sheet resistance was observed and it was concluded that no interaction occurs between Si_3N_4 and $MoSi_2$.

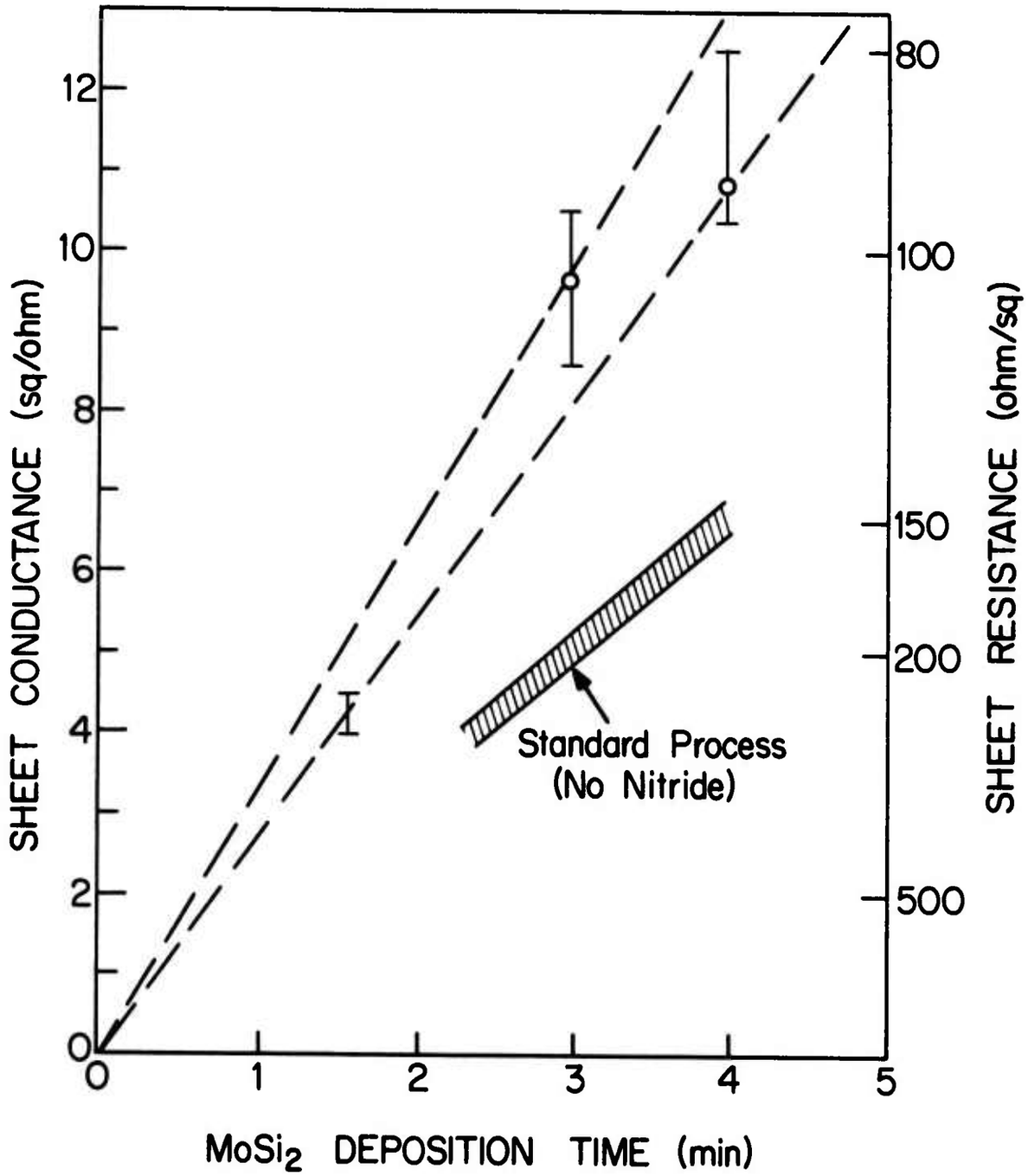


Figure 34 - Sheet Conductance versus $MoSi_2$ Deposition Time for $MoSi_2$ Under Silicon Nitride Deposited at 800°C (Engineering Line Silicon Nitride Reactor)

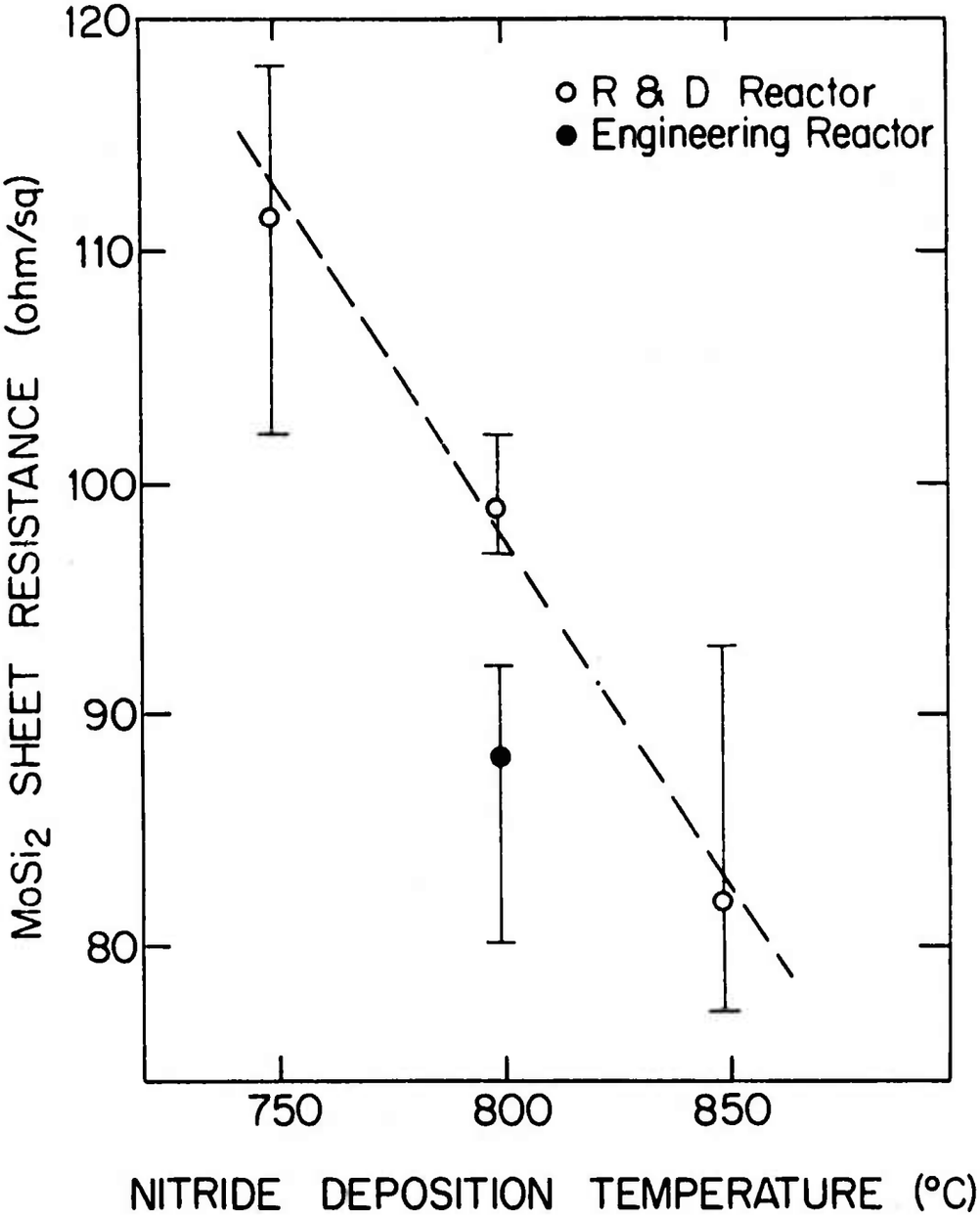


Figure 35 - Sheet Resistance of $MoSi_2$ Resistors Versus Nitride Deposition Temperature. Resistor Deposition Time is Four Minutes.

One solution to the resistor variation problem was to pre-anneal the wafers at a higher temperature than that used for the Si_3N_4 deposition. Annealing was carried at 850°C and it was found that the annealing essentially saturates within the first five minutes as shown in Table 7.

TABLE 7 TIME DEPENDENCE OF ANNEALING

Wafer #	Time at 850°C (Minutes)	Resulting Sheet Resistance Ω/Square
1	5	140
	10	140
2	5	140
	15	140
3	5	187*
	20	170*
4	5	147

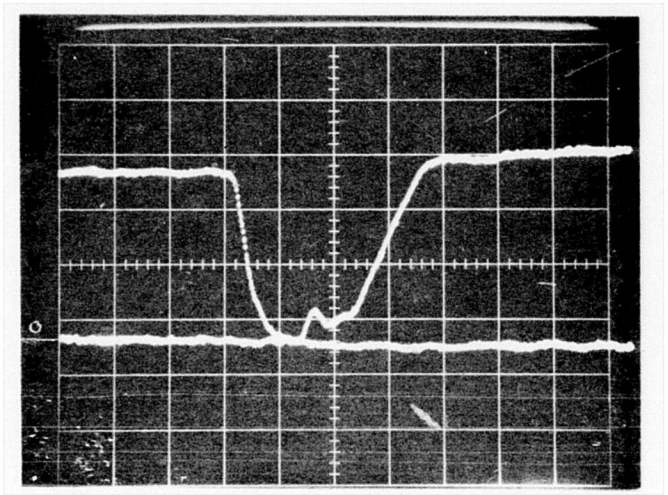
*Different initial thickness from other wafers.

The high temperature annealing accomplished its original purpose, resistor values became very uniform and resistor target values were easy to achieve. Unfortunately, however, the higher temperature is believed to have caused gold (introduced during the emitter processing step to reduce device storage time) to migrate from its former electrically active sites and precipitate at dislocation sites. If a junction is located at one of these sites high leakage currents can occur. In addition, the reduced gold concentration in the electrically active sites caused an increase in the device turn-off time. After the 850°C anneal step was introduced, device failure caused by both of these effects increased markedly. The increase in turn-off time is shown in Figure 36.

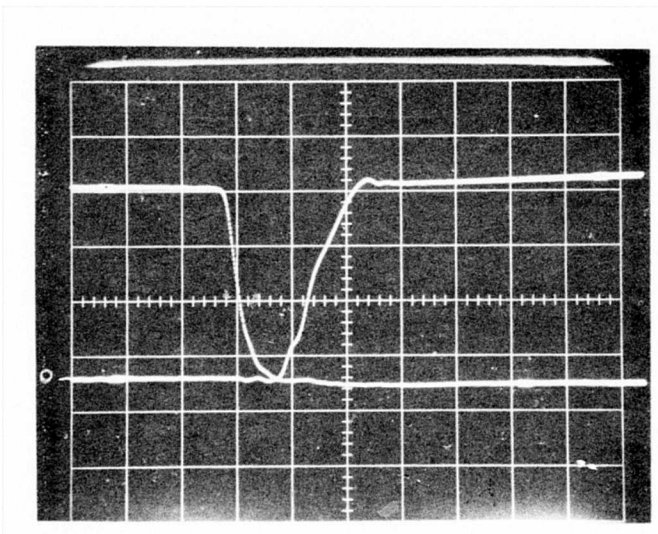
SILICON MONOXIDE PASSIVATION

An anodization resistant (passivation) material with a lower deposition temperature was sought to replace Si_3N_4 and SiO was chosen. Since SiO is deposited at essentially room temperature, it does not affect the resistor or device properties.

SiO Process: The SiO resistor passivation process is described with respect to Figure 37. Because the SiO is not easily removed by etching, a lifting process is used to define the SiO to the required pattern. The lift process uses photoresist and begins prior to SiO deposition. At this point a layer of photoresist is applied to the wafer. This photoresist is then exposed and developed using a resistor passivation mask which is designed such that the photoresist is removed only from the area where the SiO is required. SiO is then deposited by standard vacuum evaporation techniques.

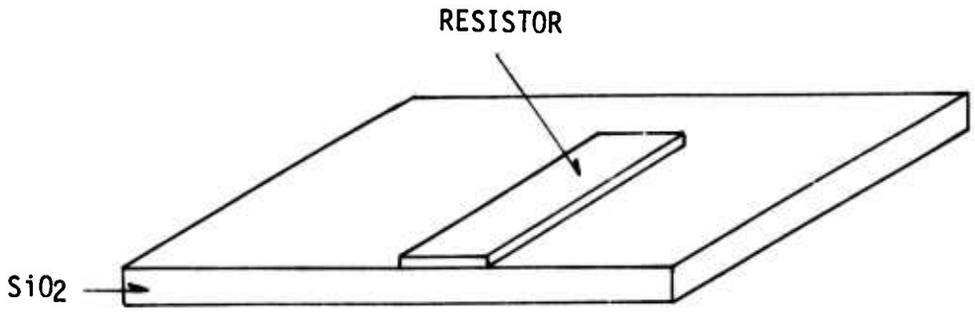


(a) Si_3N_4 Passivation, Resistor Annealing & Gold Doping

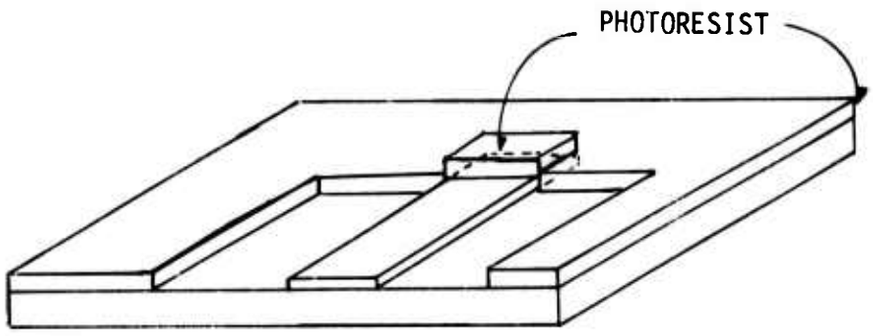


(b) Si_3N_4 Passivation & Gold Doping

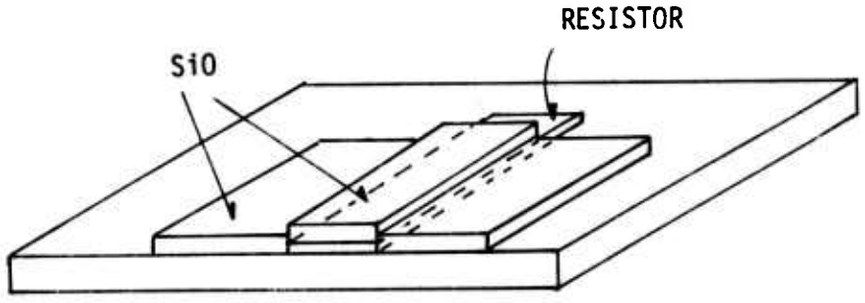
Figure 36 - A comparison between defective (a) and good (b) 9708 A-O-I devices. Note the approximate 15 nsec increase in turn-off time for the circuit which was given the 850°C resistor anneal.



(a) Initial Surface



(b) After Photoresist Delineation



(e) After SiO deposition and Photoresist removal

Figure 37 - SiO Resistor Passivation Process

In order to remove the unwanted SiO, the wafers are immersed in a solution which removes the resist material. In this case Shipley AZ-1350 is the resist material and it is dissolved by acetone. Because of the nature of the SiO deposition process, one or more sides of the photoresist will always be exposed and hence will be attacked by the solution. Under the influence of ultrasonic agitation in the bath, the resist completely dissolves and the SiO lifts off. The SiO which was not deposited on resist adheres strongly to the resistors and the oxide and remains as a sharply delineated pattern over the resistor area. Figures 38 and 39 respectively show the resistors before and after passivation, notice the open resistor contact pads in Figure 39.

Anodization Resistance: The SiO passivation capability was tested following the procedures used in testing Si_3N_4. In addition, since it might be expected that vacuum deposited layers contain more pinholes than vapor deposited layers, the pinhole density of as-deposited SiO was also determined.

The above concerns were tested directly by depositing various thicknesses of SiO over aluminized wafers. Electrical contact was made to the aluminum and the SiO subjected to the full anodization voltage (160-180 volts) in the anodization bath.

The results of this direct test of SiO anodization resistance indicates that SiO anodizes (is electrochemically attacked) at a slow rate being about 300Å/minute for a 3000Å thick SiO film. Thicker films are attacked less readily because a greater proportion of the applied voltage appears across the film itself rather than in the electrochemical process.

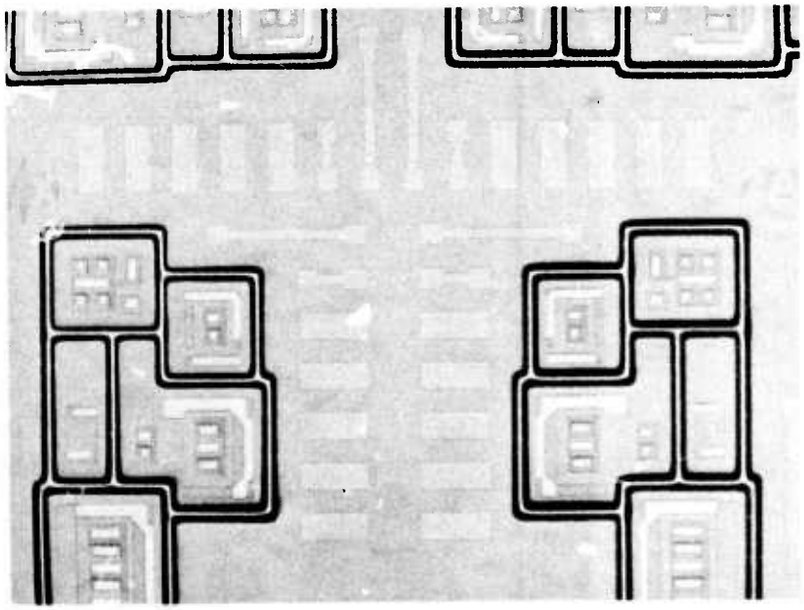


Figure 38 – $MoSi_2$ resistor before passivation.

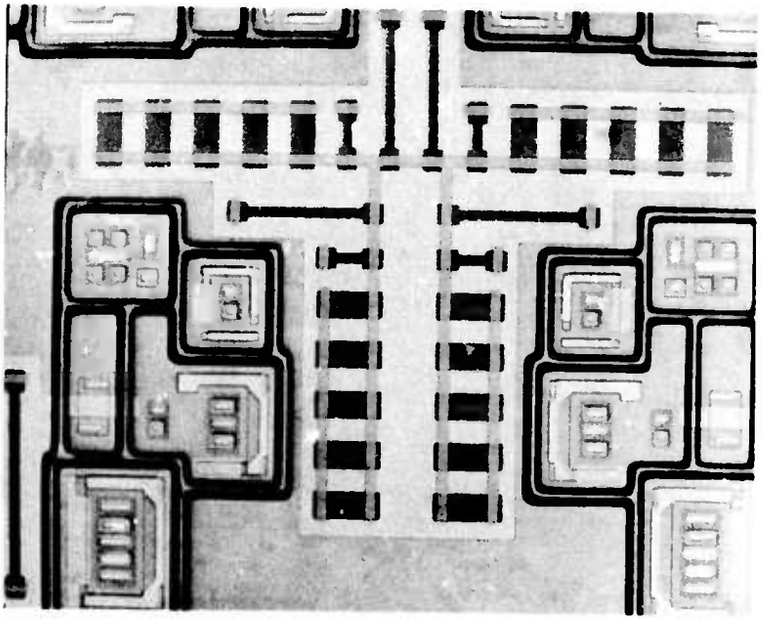


Figure 39 -Resistors passivated with SiO.

In the actual situation the SiO resistor passivation is under the aluminum to be anodized and the anodization rate of SiO is expected to be far less because the full anodization voltage will now occur across the SiO and the barrier portion of the porous aluminum oxide. Thus, it was concluded that SiO provides satisfactory protection.

The above arguments were fully tested on product wafers with SiO protected resistors. Again a direct comparison was obtained on the same wafer between areas where the aluminum was delineated by anodization and areas where the aluminum was delineated chemically (no anodization). Resistor measurements made on each portion indicate essentially no effect since on the average a resistor variation of less than 1% was observed.

The pinhole density was checked on the SiO layers which were subjected to the direct anodization. Optical inspection indicated that the density of pinholes was small and the pinholes which do occur seem to be caused chiefly by bits of lint or other foreign material on the wafer surface just prior to the SiO deposition.

CONCLUSIONS

In accordance with the objectives of this program the compatability of aluminum anodization and thin film resistors was assessed and the necessary methods of protection developed and proved out. The final process employs resistors protected with an evaporated SiO layer 3000Å thick (Figure 40). This layer performs satisfactorily in all aspects and except for some initial parts, all of the 9702 and 9708 circuits produced in this program utilize SiO resistor passivation.

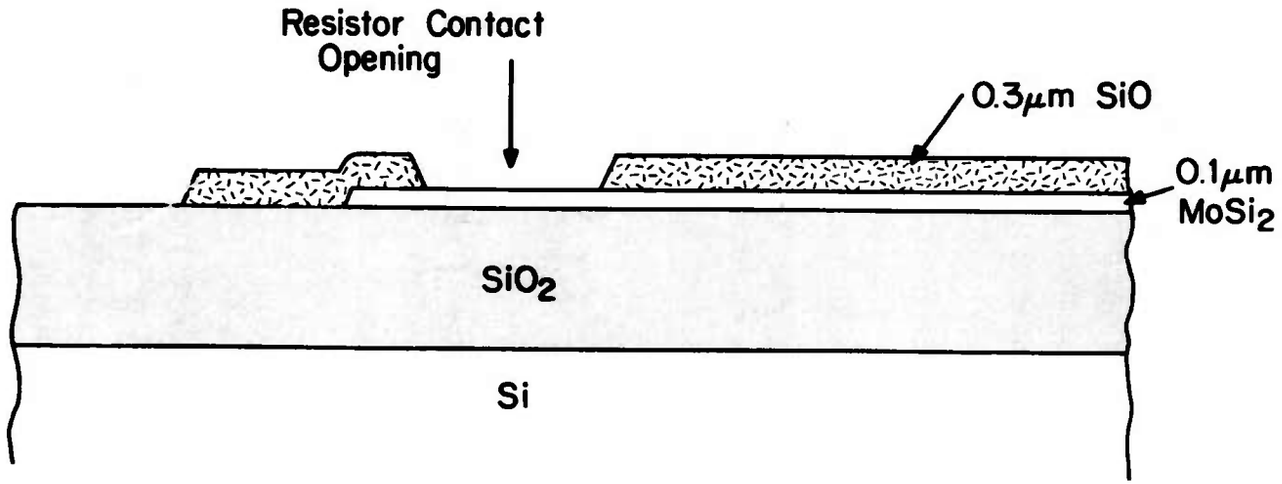


Figure 40 - Schematic Cross-Section of Passivated Thin Film Resistor.

However, it should be pointed out that the objection to Si_3N_4 was due to the inability to achieve uniform deposition temperatures because of equipment problems. With improved equipment, Si_3N_4 passivation could perform satisfactorily.

SECTION IV

ANODIZATION MANUFACTURING METHODS

INTRODUCTION

One objective of this program was to develop an anodized aluminum manufacturing process for dielectric isolated circuits and to demonstrate its feasibility by manufacturing anodized circuit dice to be used in the assembly of a multichip 6 bit adder (described in Section V). The investigations and process developments necessary for the implementation of an anodized aluminum process have been covered in Sections II and III. It is the purpose of this section to describe the final anodization manufacturing process in detail. This description includes processing methods and controls, as well as a brief description of the demonstration vehicles, the modifications necessary for anodization processing, and the development of a multiple wafer anodization station that was used in the production of the anodized circuits for the multichip 6 bit adder.

DEMONSTRATION VEHICLES

The demonstration of single layer aluminum anodization processing and its advantages was made using the Fairchild 9708, a four-wide 3-2-2-2 input, and/or invert gate, and the Fairchild 9702, a quad two input Nand gate. These circuits are part of Fairchild's radiation-hardened TTL circuit family, (The circuit diagrams are given in Section V). These circuits, as originally designed and produced, utilized the following radiation hardening techniques: Dielectric isolation, Ni-Cr thin film resistors, all aluminum metallization, thin film resistor photocurrent limiting, and thin film resistor passivation and scratch protection.

In order to prepare these circuits for anodization, the following modifications were made. The thin film resistor process was changed from Ni-Cr to $MoSi_2$. The primary reason for this change is that $MoSi_2$ is thicker and therefore can more reliably withstand high temperature processing and exposure to etchants or electrolytes. The anodization process requires that the resistors be protected and hence, a mask was fabricated to open the resistor contact through the protective passivating layer. In addition to this, a special mask was fabricated which connected the scribe line to the metallization pattern, and another mask was fabricated to remove this connection after the anodization was completed. In summary, $MoSi_2$ was substituted for NiCr, and three masks were fabricated, the resistor passivation mask, the scribe line connection mask and the scribe line severance mask. As has been pointed out in Section II, the last two masks are not necessary if the aluminum is of good quality. Finished anodized 9702 and 9708 dice are shown in Figures 41 and 42.

The dual layer metal anodization demonstration vehicle, the 9780 four bit shift register, has been described in sufficient detail in Section II. This circuit as developed already employed passivated $MoSi_2$ resistors. For a two level metal circuit, no additional mask changes are necessary in addition to those required for one level metal processing as described in the previous paragraph.

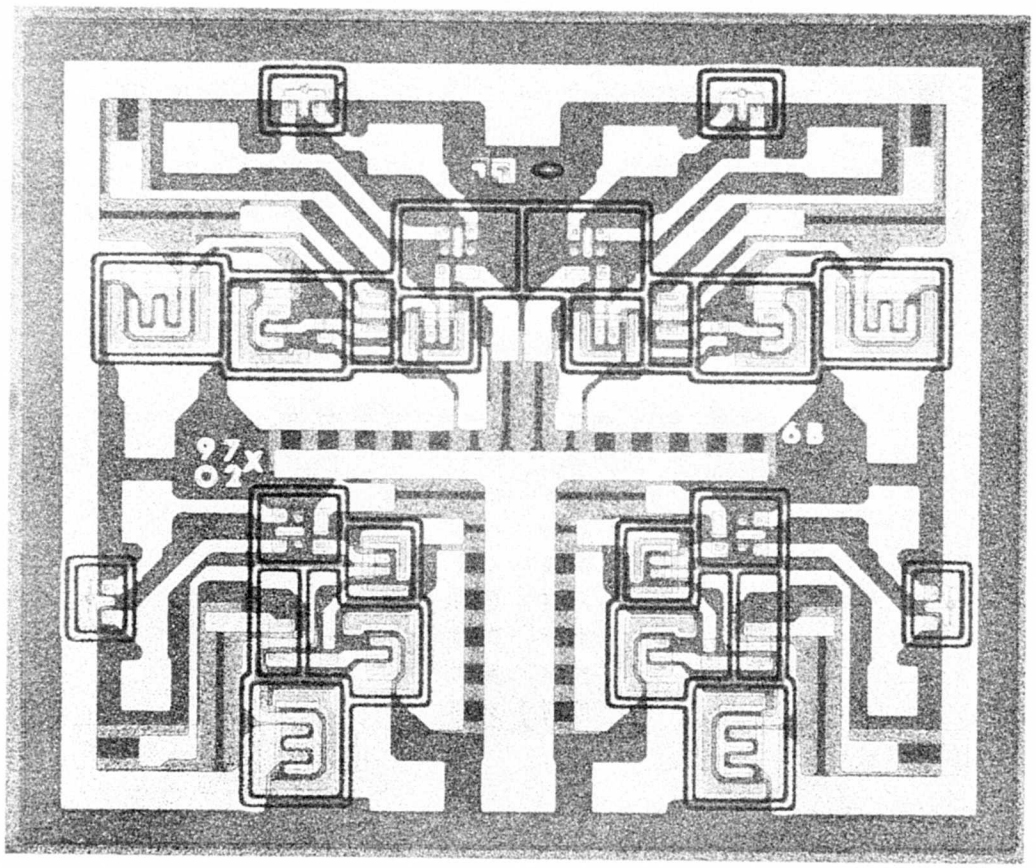


Figure 41 - An Anodized 9702 Die.

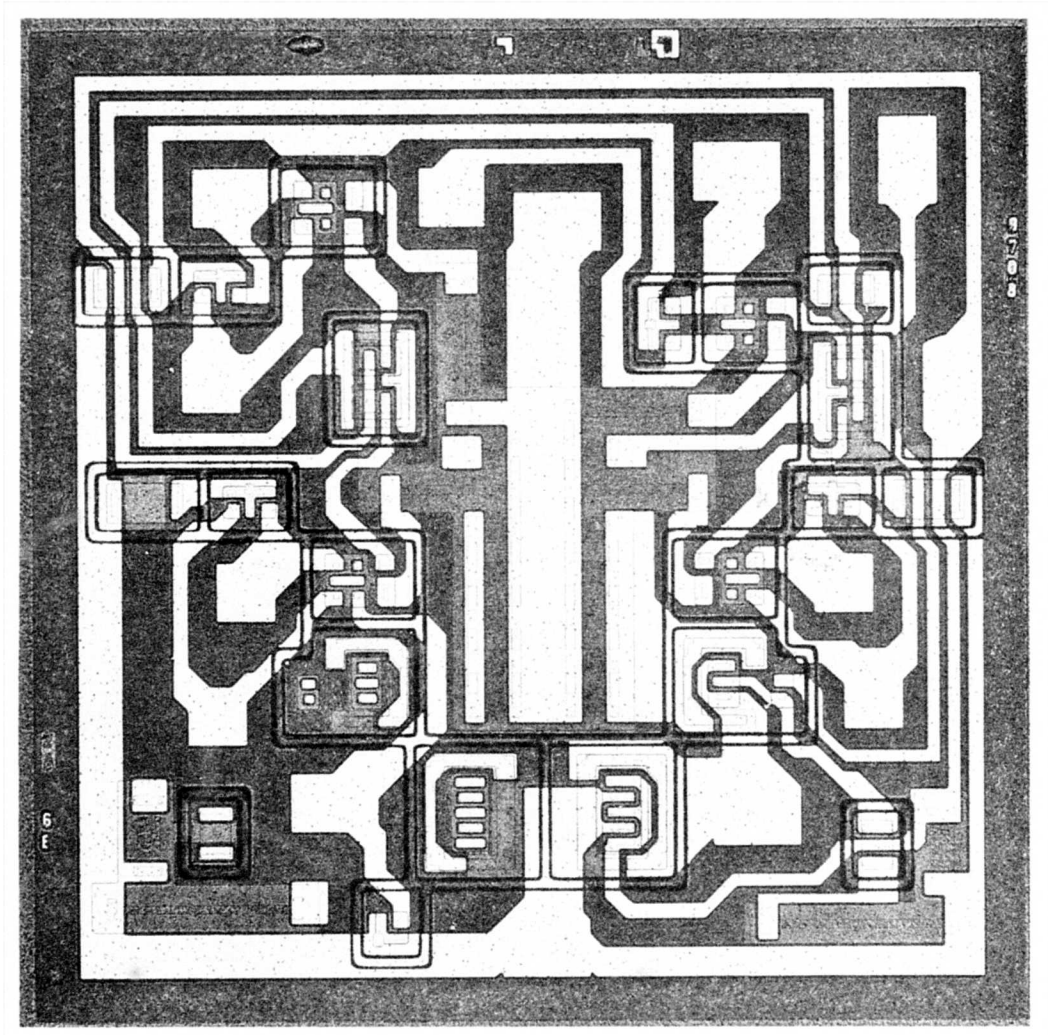


Figure 42 - An Anodized 9708 Die

MULTIWAFER ANODIZATION PROCESSING STATION

Multiwafer Holder-Considerations and Design

Except for very low volume production, it is required that the manufacturing process developed be suited to volume processing. In developing a multiwafer anodization cell a number of considerations must be taken into account. These are dictated primarily by (a) the need to electrically contact and hold each wafer in a stirred electrolyte, (b) the geometrical effects on anodization and (c) electrolyte temperature control. Electrolyte temperature control can be achieved either by inserting cooling or heating coils in the anodization bath or by immersion of the cell in a constant temperature bath. The other considerations are more involved and will be discussed in some length.

Making good electrical contact to the wafers is not a simple problem. The simplest way is to clip the wafer and hold it only partially immersed so that the clip does not itself contact the electrolyte. This is unsatisfactory because, since the electrolyte is stirred, a sizeable fraction of the wafer is not processed. Furthermore, reproducibility of the anodization is affected and, if high anodization voltages are used, sparking can occur at the point where the electrolyte-air-metal interfaces meet. If the wafer is completely immersed, the requirement placed on the contacting method is that current loss from the clamp assembly to the electrolyte be small compared to the total anodization current. To give an extreme example, if a gold or platinum wire were used to contact the wafer, current loss from the wire to the solution could be so high that very little aluminum anodization would occur. The literature on anodization describes many contacting methods developed to minimize current loss to the electrolyte.

The importance of contacting is discussed in Young's book.[6] Fairchild's investigation over the past years of the anodization of silicon, silicon nitride and aluminum has also developed a number of contacting schemes. These include contact to the wafer backside using a wire spring[7] or mercury[8]. In each case, the wafer is held by a vacuum jig and a rubber seal is made between the jig and the wafer. This seal protects the wire spring or mercury from the solution. This type of approach can be made to work but there may be difficulty in repetitively making a good vacuum seal. With radiation hardened devices, the situation is worse because the polycrystalline silicon is rough and, hence, it is necessary to polish this surface in order to hold a vacuum. A better approach is to used an insulating clamp with a wire point contact. This type of clamp (Fig. 43, See also Fig. 25, Section II) has been used at Fairchild since early 1970 in the investigations of aluminum anodization.

Geometrical considerations primarily involve the respective positioning of anode (wafer) and cathode during anodization. The most frequently used arrangement is to place the anode and cathode at some distance and parallel to each other. This is done to ensure that the voltage drop in the electrolyte due to the current passed is the same to all points of the anode. If this is the case, the anodization will proceed uniformily over the wafer. If this is not the case, then certain areas of the wafer will clear first and can lead to incomplete anodization of other areas. The amount of non-uniformity depends primarily on electrolyte conductivity. The electrolytes used in the present processes are fairly conductive and the effects caused by non-parallelism are small.

In designing a multiwafer holder, there are two obvious ways of meeting the geometrical requirements. One method is to closely space wafer, cathode, wafer, cathode, etc., in succession. In this

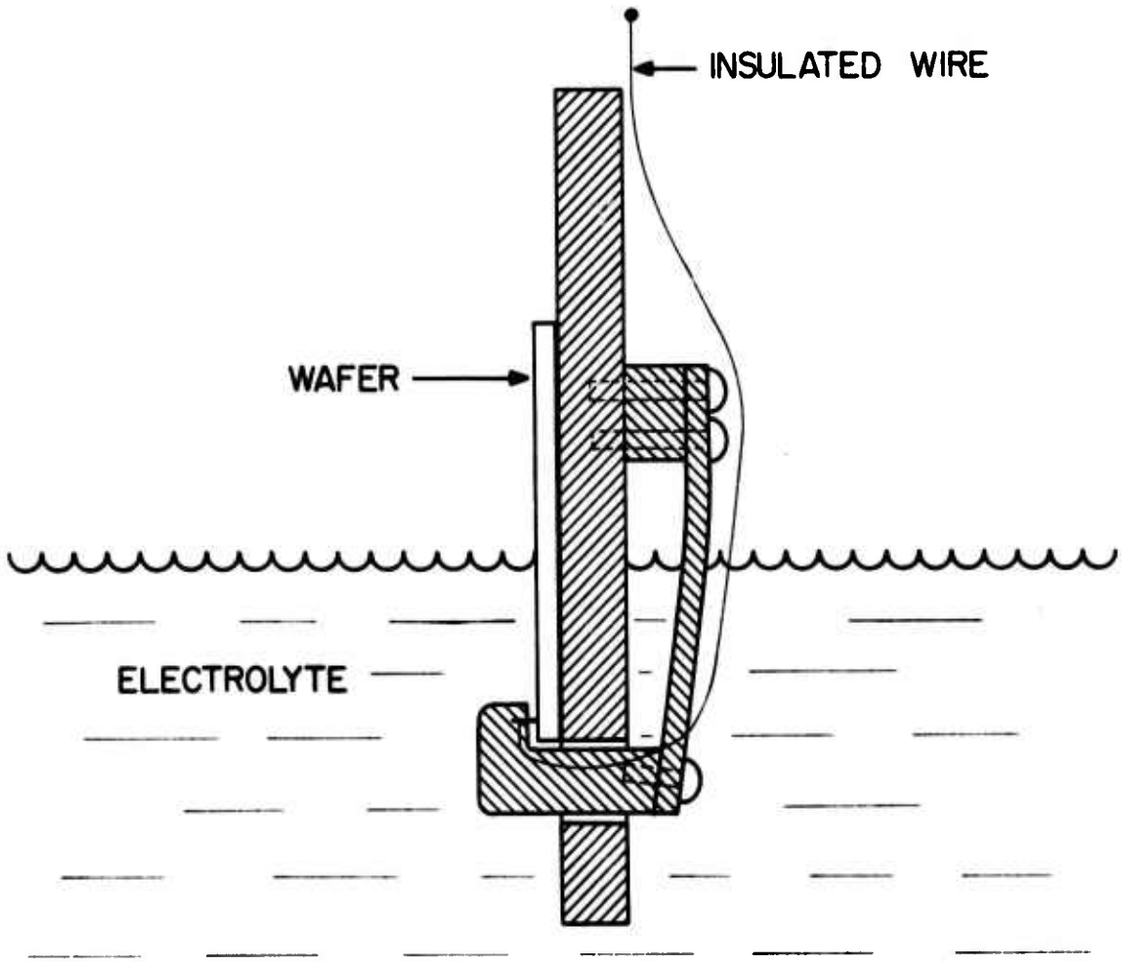


Figure 43 - Schematic Cross-Section of an All Plastic Anodization Clamp (Shown in the anodization of a partially immersed wafer for a specific experiment described in Interim Report #3).

case, the electrolyte can be agitated by stirrers placed on the side such that the liquid is forced across the wafer surfaces. Another method is to place all wafers in the same plane opposite one common cathode. Stirrers, in this case, can be placed between the cathode and anode planes. The last method has the advantage that the anodizing wafers may be easily observed and this approach was taken here.

A front and rear view of the multiwafer holder is shown in Figures 44 and 45. The holder is constructed from inert plastic materials and basically consists of eight clamps of the form shown in Figure 43. These clamps serve to hold and make an electrical point contact to the wafers during anodization. The insulated wire used for point contact in each clamp is connected to a bus wire (Figure 45) which distributes current from the power supply.

The holder will handle eight wafers up to 2-5/8" in diameter. However, in the present case, 2" diameter wafers were used for the radiation hardened integrated circuits. The clamps can be lifted or applied to the wafer by rotating an off center shaft (C in Figure 45 using lever B. The shaft pushes the plastic spring levers A, thus causing the point contacts to lift from the front of the holder. This design meets one further criterion, the ease of placing and removing wafers.

Processing Station:

The processing station consists of the following items: a cell in which the multiwafer holder is placed, a cathode consisting of a sheet of perforated aluminum, motor driven paddles to stir the electrolyte, a constant current power supply equipped with a voltage limiter to supply the anodization current, and a voltmeter and

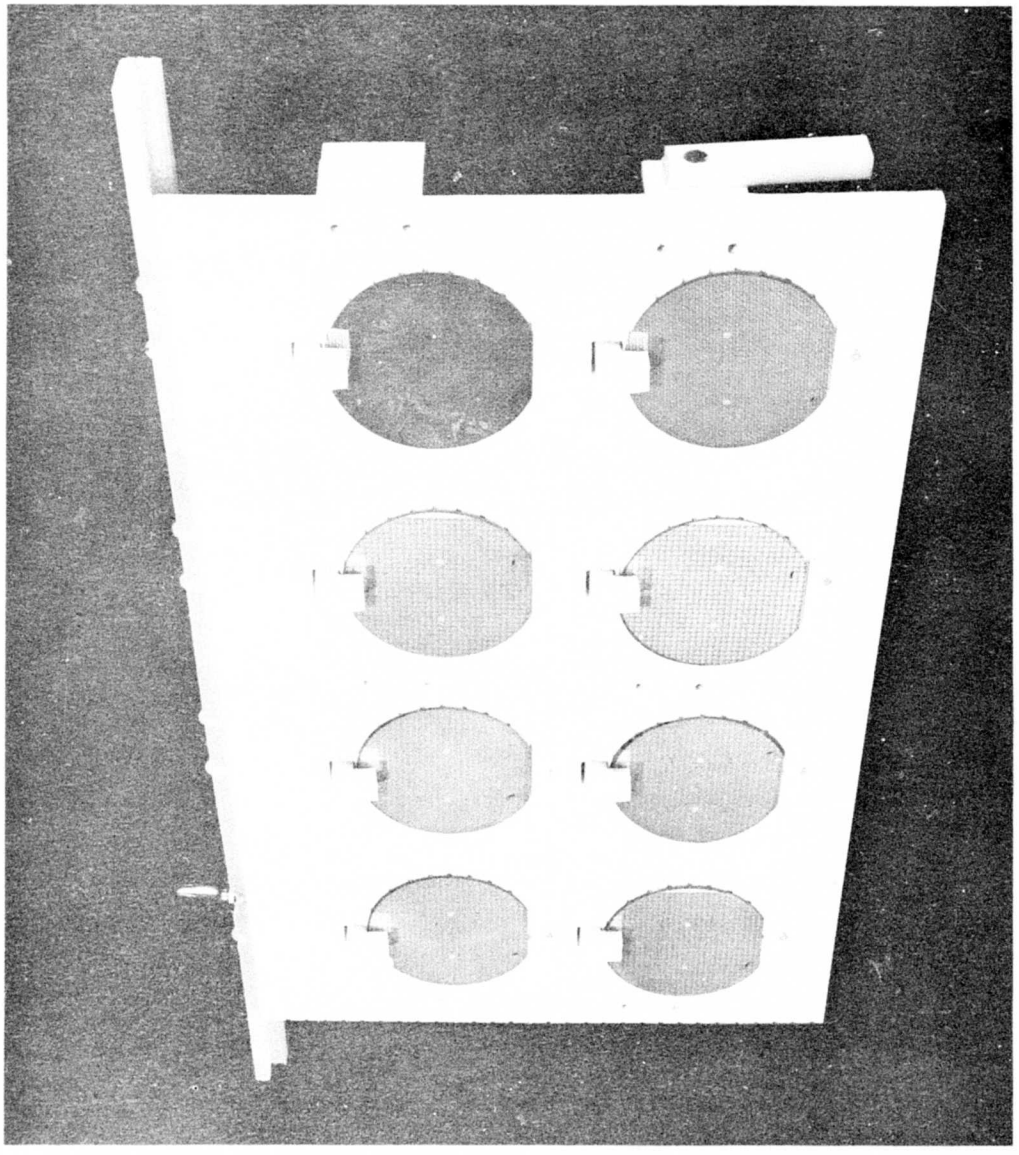


Figure 44 - Photograph of multiwafer holder after anodization of eight two-inch diameter wafers.

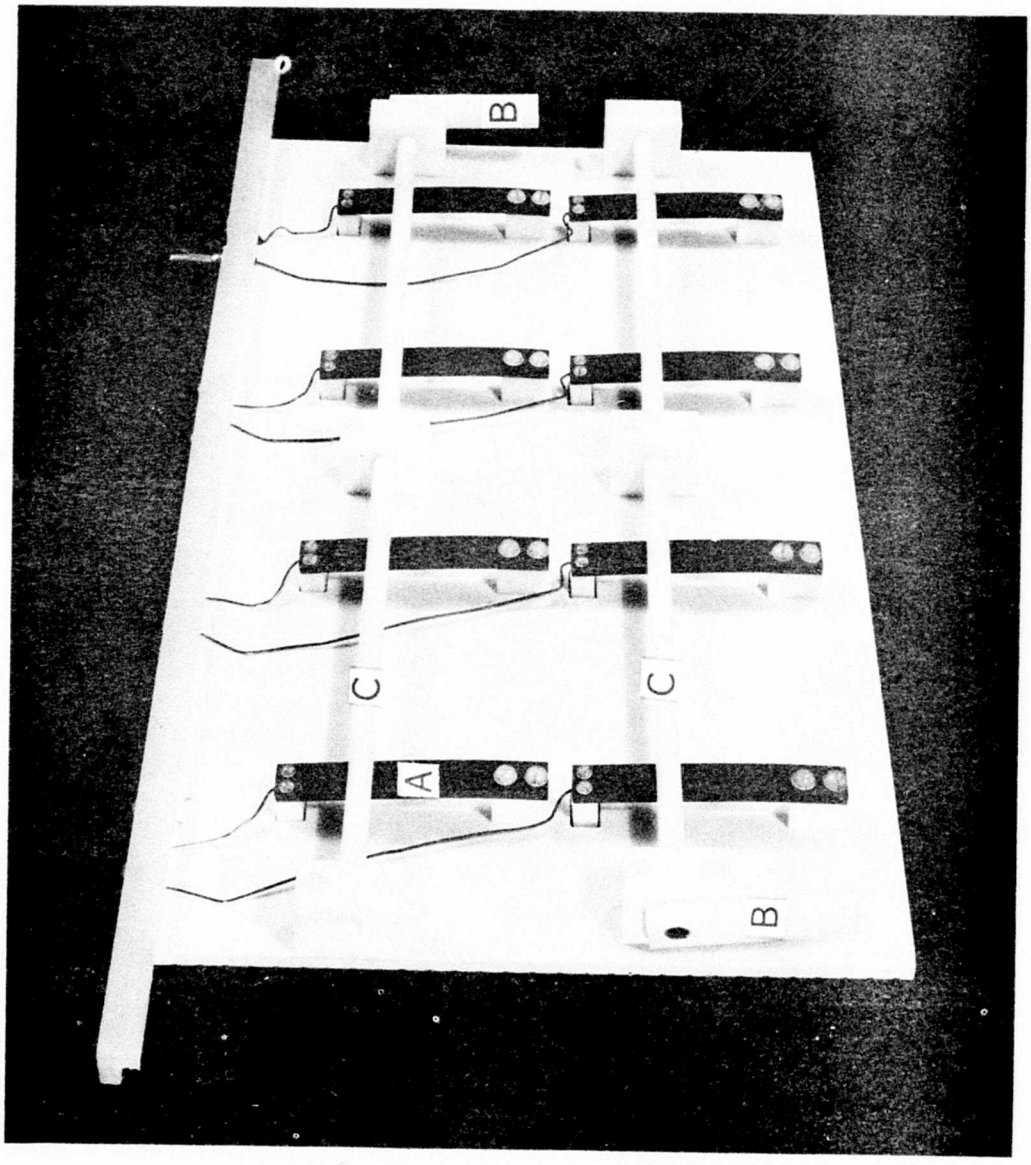


Figure 45 - Photograph of rear of multiwafer holder showing how clamps of the type in Fig. 3 are arranged.

chart recorder to monitor the anodization progress. The cell is immersed in a constant temperature bath to maintain the electrolyte at a prescribed temperature. The apparatus is situated next to wet hoods used in preparation of wafers for anodization.

FABRICATION PROCESS

The radiation hardened circuits to be anodized were fabricated using Fairchild's single poly dielectric isolation process up to the point where all device diffusions were complete and contact openings were etched to the active device areas. The description of the final anodization process begins at this point and is summarized in Table 8 for single layer metal circuits and in Table 9 for dual layer metal circuits.

Single Layer Metal Anodization Process:

With respect to Table 8 the process details are as follows:

1. Open Contact Windows: This is a standard process utilizing photoresist masking and etching to form openings in the oxide over active device areas in order to contact the devices with the aluminum that is later deposited. After contact etching is complete, the wafers undergo optical inspection in order to check that the contacts are clean and not over or under etched. Some test devices are electrically probed to ascertain that the devices possess the desired characteristics. If the results are satisfactory, the wafers are processed further.

2. Resistor Deposition And Lift: The $MoSi_2$ resistor process is described in Section III. Very briefly, the resistors are delineated by a lift process which requires that a pre-patterned

TABLE 8

Final Process Sequence for Anodized 9702 and 9708 Single Layer Metal Circuits. Process begins After Emitter Diffusion.

	Processing Steps	Process Monitor
1.	Open Contact Windows	Optical Inspection & Device Check
2.	Resistor Deposition and Lift Process	Optical Inspection & Resistivity Check
3.	SiO Deposition & Lift Process	Optical Inspection
4.	Aluminum Evaporation	Monitor Evaporation Conditions, Thickness, and Anodization Quality
5.	PVx Deposition on Al	PVx Thickness and Etch Time
6.	Define PVx to the Metal Pattern	Optical Inspection
7.	PVx Deposition on Wafer Backside	
8.	Porous Anodize	Optical Inspection
9.	Open Contact Pads in PVx	Optical Inspection
10.	Aluminum Alloy	
11.	Electrical Wafer Sort	

layer be formed on the wafer surface prior to $MoSi_2$ deposition. This layer covers everything except the intended resistor areas. After depositing $MoSi_2$, the pre-formed layer is etched away, thereby removing the unwanted $MoSi_2$ and leaving the resistor in place. The resistor could also be etched, however, this would require either protecting the phosphorous doped oxide glass (formed in the emitter process) on the wafer or removing this oxide. In the present case it was decided to keep the glass and to define the resistors by lifting.

The resistor deposition is carried out by sputtering in a magazine fed sputtering system. The target is 200Ω/□ and the process is monitored by including some test wafers and determing the sheet resistivity on these test wafers. After the resistors are deposited and lifted the wafer is optically inspected to ensure proper resistor definition. Figure 38 of Section III shows the 9702 die with the resistors in place.

3. SiO Process: The SiO process is described in detail in Section III. Briefly the SiO is defined by lifting (Figure 37 using a photoresist layer. While this process worked well with the 9702 and 08's, in the 9780, the AZ 1350J* resist adhered poorly to the contact and in many cases disappeared completely after development. Investigation indicates that the decreased adhesion occurs because the area protected by photoresist is approximately a factor of 8 less in the 9780 than that of the 9702 or 9708's (Figure 46). Since the resist adhesion is mostly of a mechanical nature, reducing the area reduces the total adhesion strength. The problem was overcome using a different photoresist, AZ 111*. However, because there are more resistors in the 9780 than in the 9708

* Manufactured by Shipley

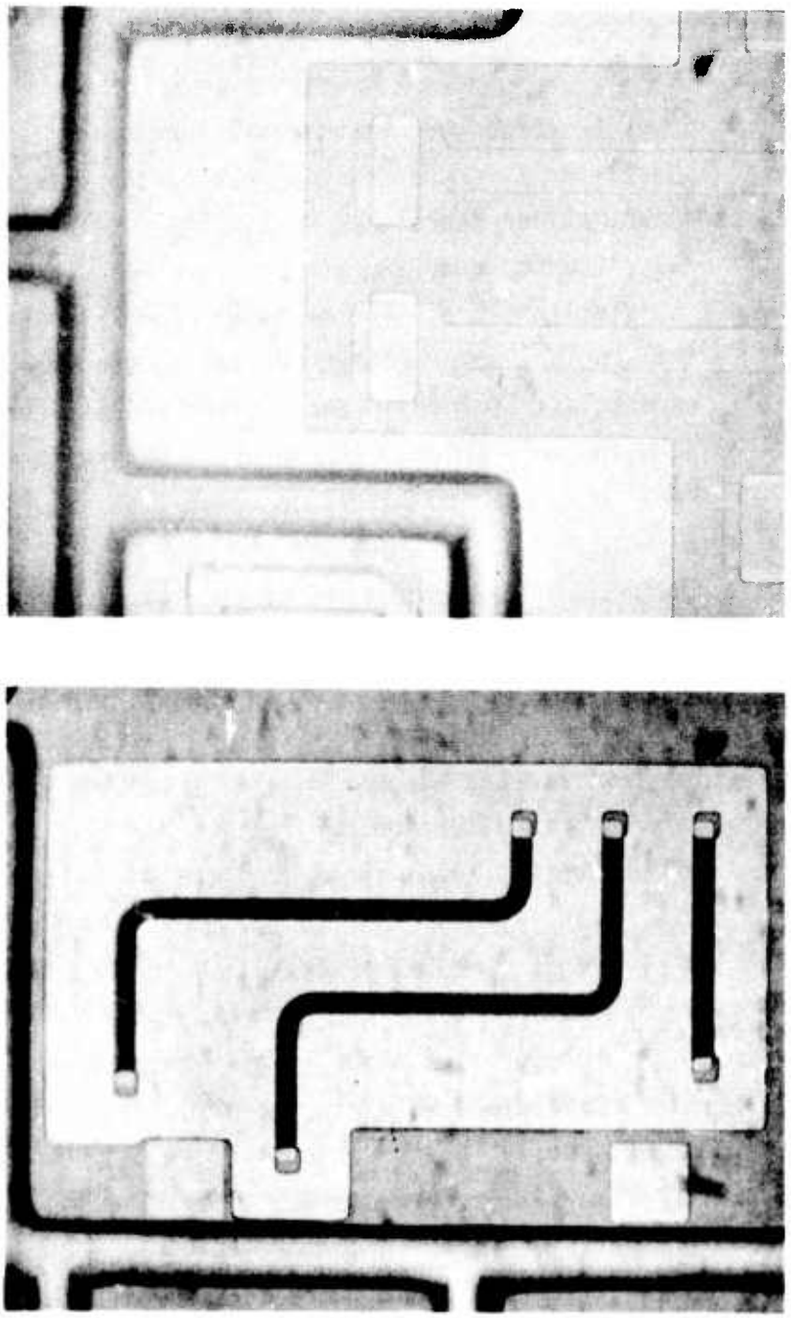


Figure 46 - A comparison between the resistor contact area size for the 9702 circuit (above) and the 9780 circuit (below).

or 02 circuits, unopened contacts was a common failure mode for the 9780 circuit. In the future, this problem can be circumvented by proper design of resistor ends and contacts. At the present time, the process is monitored by optical inspection after delineating the photoresist lift pattern. If the inspection reveals uncovered contact areas, the photoresist is removed and the wafer reworked until proper contact coverage is obtained.

4. Aluminum Evaporation: The aluminum evaporation is very important to the success of the anodization. Following the results in Section II, the aluminum is deposited by electron beam evaporation of 99.999% aluminum. The deposition is monitored with a Sloan thickness monitor and the nominal thickness is 1.2μ ± 10%. In order to obtain good step coverage, the wafers are heated to about 350°C during deposition. The bell jar pressure is very important and should be maintained in the low 10^{-6} torr range during deposition. Pressures in the 10^{-5} torr range will give aluminum with poor clearing quality.

An evaporator may be characterized as to aluminum quality by monitoring the anodization curves. This is done by depositing aluminum on an oxidized wafer. The aluminum is covered with a layer of PVx which is masked and etched to expose a rectangular $5cm^2$ aluminum area in the center of the wafer, as well as, an area for electrical contact near the periphery. The aluminum is then anodized at $10mA/cm^2$ in 4% H_3PO_4 with the $5cm^2$ area held in the electrolyte and with the contact area out of the electrolyte. If the anodization curve is as in Figure 13 the aluminum is acceptable. If the curve deviates from this, as is the case in Figure 14, the aluminum

is not acceptable and the evaporation conditions must be improved. This type of test should be done on a regular basis.

5. PVx Deposition on Aluminum: This is a vapor deposition of silicon dioxide by the oxidation of silane gas at approximately 400°C. The oxide is doped with about 6% by weight phosphorous; however, undoped oxide works just as well. The oxide thickness was typically 0.5μ ± 10%; however, a range of 0.3 to 0.7μ can be tolerated and still maintain good surface planarity after anodization. A test wafer is included with each deposition and the resulting PVx thickness measured using an interference spectrometer.

6. Define PVx to the Metal Pattern: Standard photolithographic procedures are used to expose the photoresist to the desired metallization pattern. The resist used is KTI* having a viscosity of 80 cs and spun on at 4000 rpm. Exposure time is 0.5 sec at a light intensity of 1.0 millwatts per cm^2. The photoresist viscosity and exposure conditions have been chosen to minimize pin holes and still achieve good resolution. After development, the wafers are optically inspected for pattern resolution and then etched in a PVx etchant which is a commercially available buffered HF solution. Since the PVx thickness varies slightly over the wafer surface and from wafer to wafer, the wafers are over etched by approximately 20% to assure that the PVx is completely removed from all portions of the surface. The approximate etch time is obtained from etching the PVx on the test wafer used in Step 5.

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* Manufactured by Kodak

7. PVx Deposition on Wafer Backside: A non-critical PVx deposition (0.5μm to 1.0μm) is made on the wafer backside. Its purpose is to insulate the back of the wafers during anodization. If this were not done, current loss would occur to the electrolyte and this, in turn, would prevent proper anodization of the frontside aluminum under the required conditions. The current loss occurs through the wafer backside since it is directly connected to the aluminum in contact with the open scribe lines.

8. Porous Anodize: This is the actual aluminum delineation step and is carried out using the multiwafer anodization station. The clamps on the multiwafer holder are lifted, the wafers loaded and clamps lowered to contact and hold the wafers. Oxidized wafer blanks are used to fill any unused clamps; thus, the multiwafer holder can be used to anodize any number of wafers up to eight. The wafers are nudged slightly sideways and back in the clamp in order to ensure that proper electrical contact is made. The holder and the wafers are rinsed in deionized water and placed in the anodization cell that is immersed in a constant temperature bath at $25^{o}C$.

   The anodization is carried out at a current density of $10mA/cm^2$ of exposed aluminum. This corresponds to about 120mA per full wafer for 9702 and 9708 circuits. The total current required was estimated in each case depending on the number of wafers and partial wafers being anodized. The current was raised to its full value over a period of about twenty seconds. For $10mA/cm^2$ the peak voltage should be around 150-155 volts and the operating voltage should be 130-140 volts. Proper peak and operating voltage is an indication of proper current density. The

anodization typically will near completion in five to six minutes at which point the voltage rises to a preset 160 volt limit and the current rapidly falls off (see, for example, Figures 7 or 13, Section II). The anodization is continued until the total anodization time reaches twelve minutes. Power is then disconnected, the wafer holder removed and the wafers demounted.

The anodization solution used is 4% by volume of concentrated H_3PO_4. The solution is agitated by two motor driven paddles. The temperature of the solution should ideally be 25^oC, however for a full complement of wafers, the temperature rose several degrees without any noticeable affect on the anodization. The anodization solution is not significantly depleted by use but is usually replaced because of evaporation losses or suspected accidental contamination.

The wafer holder is placed such that wafers may be observed during anodization. The wafer surface remains reflecting until the anodization nears completion. The beginning of completion is signaled when some small area on the wafer darkens (becomes less reflective). This area widens and in a matter of twenty or thirty seconds engulfs the entire wafer at which point anodization is essentially complete.

After the anodization is completed, several wafers are inspected microscopically to assess the quality of the anodization. Although difficult to describe, with some experience it is possible to determine if the anodization is satisfactory or unsatisfactory. An unsatisfactory anodization has been found to occur only for two reasons: insufficient etching of the PVx layer or poor quality aluminum. Insufficient etching of the

PVx results in spotty or no anodization. This can generally be detected with the unaided eye and can be remedied by placing the wafer in the PVx etch solution a little longer and then re-anodizing the wafer. Poor quality aluminum can only be remedied by reworking the wafer. This means removing the PVx, the Al_2O_3 and the Al, and starting over again at aluminum deposition. Although wafers can be reworked several times without any adverse effects, this can be avoided by exercising proper control over aluminum quality.

In general, the anodization station worked satisfactorily and reliably. Some maintenance is required, the electrical contacts must be cleared of oxide daily. This is done by passing a piece of emery paper under the closed clamp and rinsing away any residue. Of course, the nominal clean handling procedures should be used in handling the multiwafer holder, the electrolyte and the wafers. Because of power supply limitation, four wafers were usually anodized simultaneously. However, eight wafers have been anodized a number of times at reduced current densities. The results were satisfactory and indicate that this multiwafer process could easily be scaled to handle more wafers.

9. Open Contact Pads in PVx: The wafers are masked with photoresist and the PVx over the contact pad areas is removed to expose the aluminum for electrical probing or to facilitate external electrical connection.

10. Aluminum Alloy: The aluminum is alloyed to ensure good electrical contact to the active and passive devices on the die. The alloying is performed in a nitrogen furnace at about $500^{o}C$ for 10 minutes.

11. Wafer Sort: Each circuit on the wafer is automatically probed and electrically tested to determine the good die yield or conversely to determine the cause of a poor yield. Circuit fabrication is complete at this point and the wafer is now, for example, ready for the aluminum bump or beam lead fabrication processing that is required for multichip assembly, or ready for separation into dice and die assembly. The final single level metal structure is shown in Figure 47.

Marginal Aluminum Quality

If the aluminum quality is marginal it is necessary in step 6 (Table 8) to employ the scribe line connection metallization mask rather than the ordinary metallization mask. It is then necessary to add a step that removes this connection after anodization is completed. This step is inserted between steps 8 and 9 (Table 8) and it consists of photoresist masking and then etching the PVx and the Al connecting the circuit as well as in the scribe line. This process was carried out with the aluminum received from one of the evaporators used in this program. The process was found to be feasible for manufacturing and was reproducible. The aluminum quality from this evaporator was marginal and connecting the scribe line made the difference between very poor and very good circuit yield.

1. [illegible]
2. $MoSi_2$ resist[illegible] 5
3. SiO resistor passivation

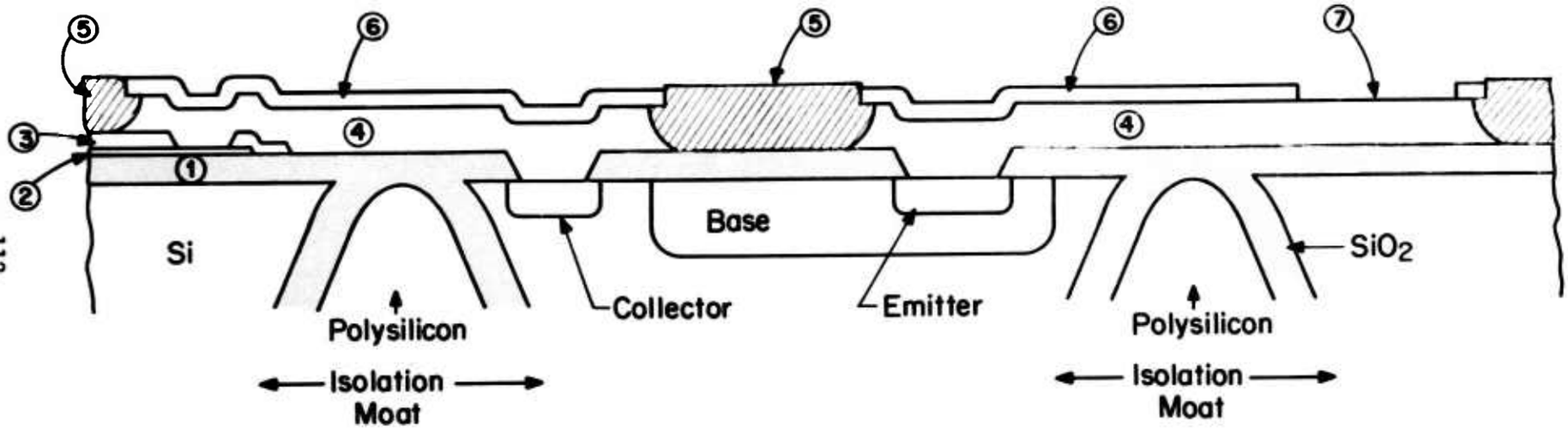


Figure 47 - Schematic cross-section of anodized single level metal structure of a radiation resistant circuit that was fabricated by the single poly dielectric isolation process.

Two Layer Anodization Process:

The two layer metal anodization process follows the single layer metal process in every detail up to and including step 8 of Table 8. The remaining steps after this point are shown in Table 9.

TABLE 9

Final Process Sequence for 9780 Dual Layer Metal Circuit

	Processing Steps	Process Monitor
a.	Steps #2 to 8 of Table 8	Monitors for Steps #1 to 8 of Table 8
b.	PVx Deposition	PVx thickness and etch time
c.	Open vias	Optical Inspection
d.	Aluminum Evaporation	
e.	2nd Metal Delineation	Optical Inspection
f.	PVx Deposition	PVx thickness and etch time
g.	Open contact pads in PVx	Optical Inspection
h.	Aluminum Alloy	
i.	Electrical Wafer Sort	

With respect to Table 9 the process details starting with step b are as follows:

b. PVx Deposition: This process is exactly the same as in Step 5, Table 8. The resulting PVx thickness is about 1μ above first level metal and about 0.5μ over the porous oxide.

c. Open Vias: Vias are openings etched in the PVx insulation in order to form contact areas between first and second level metal. The vias are formed by standard photoresist masking and etching. This is a standard process in dual layer metal and no problems were encountered in successfully opening the vias.

f. PVx Deposition: A final layer of PVx (∿.8μ) is deposited to protect the second layer metal.

h. and i. are the same as 10 and 11 in Table 8.

The two layer process has been found to work satisfactorily. In particular, it was observed that problems encountered with standard dual layer metal processing were minimized and a definite yield improvement was observed through the metallization steps. The reason for this is that in standard processing, because of less desirable surface profile, it is very difficult to form the second layer metal. If the second level metal is unacceptable the wafer is lost because rework is generally not possible. This is because the second level metal cannot be removed without removing or severely thinning the 1st layer metal under the via. Therefore, it is necessary to remove the PVx and the first layer metal and start over again at first metal. However, the PVx layer cannot be removed without damage to the device oxide. Thus rework of standard dual layer wafers is almost never done and these wafers are lost. With anodization, this loss is minimized. The resulting dual layer metal structure is shown in Figure 48.

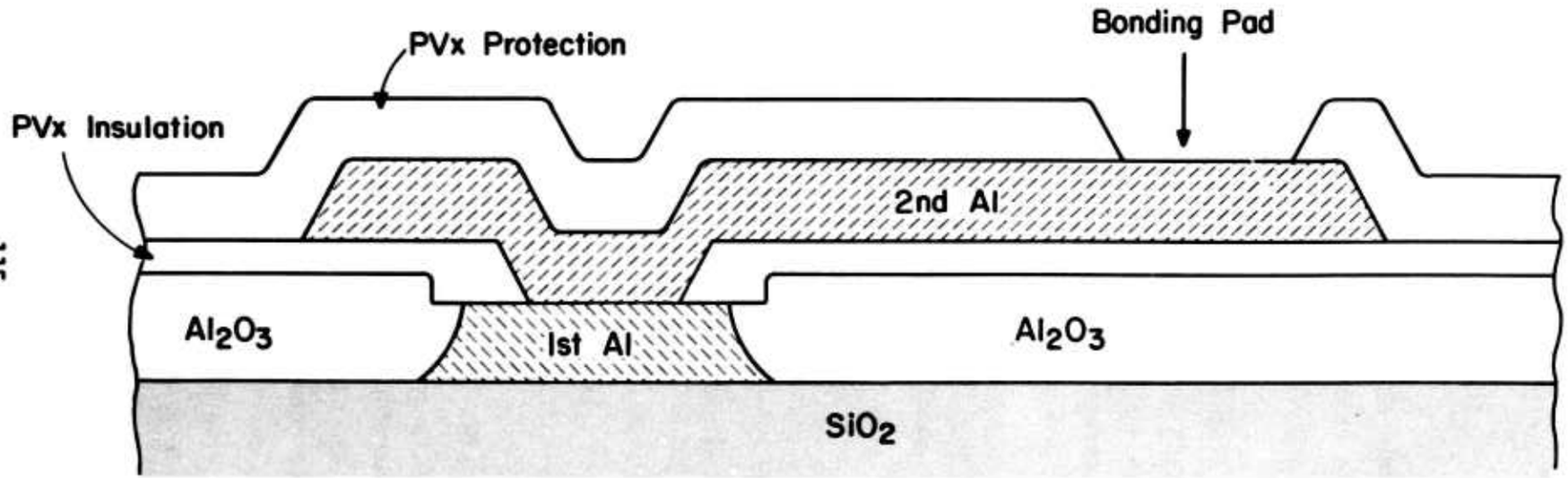


Figure 48 - Schematic cross-section of anodized two level metal structure.

SECTION V

MULTICHIP PACKAGE ASSEMBLY

INTRODUCTION

The last major objective of this program was to fabricate radiation resistant, high density, multichip assemblies contained in a hermetically sealed package. The multichip assembly was made by first forming aluminum beam leads or aluminum bumps on radiation resistant gate circuits and then bonding these circuits to preformed aluminum interconnections on a ceramic substrate. The purpose of this section is to describe the application of the multichip technology to the fabrication of a Six Bit Adder.

The state-of-the-art for multichip packaging technology will first be reviewed and then the advantages to be gained from the technology will be discussed. A description of the test vehicles, the aluminum bump and beam lead processes, and the development of a hermetically sealed multichip package will also be presented together with a discussion of the results obtained from this manufacturing methods program.

COMPARISON OF MULTICHIP ASSEMBLY METHODS

Integrated circuit components and subsystems for many types of military applications including systems exposed to radiation have for the most part been assembled by chip and wire technology. Typically with this technology, semiconductor chips are first attached to substrates or packages. The chip terminals are then electrically interconnected with other chips or with the substrate metallization pattern or with package leads by means of wire bonds using gold or

aluminum wire. If a multichip substrate is used it must also be attached to a package and more wire bonds are needed to connect substrate terminals and internal package leads.

The chip and wire technology has two major weaknesses. First, the large number of wire lead bonds required for multichip circuits results in increased probability of circuit failure due to defective bonds. Secondly, mechanical failure of the wire bonds and wire, die attach, substrate attachment and other package failures can be induced when the circuit is subjected to a spalling threshold environmental test.

The first weakness can be partially alleviated by using a leadless die attach to the substrate. In this case the bonds can be formed by the use of raised protrusions, or bumps on the surface of the chips, (Fig. 49), or by the use of metal extending from the periphery of the chips, i.e., beam leads (Fig. 50). The die are then inverted, hence the term "flip-chip", and the bumps or beams are simultaneously bonded to the substrate metal in order to achieve the desired connection. When bumps are used, the clamping force for bonding acts on the chip itself, while for beam leads the clamping is done on the beams and does not affect the chip. Such bonding can be achieved by thermo-compression, soldering, or ultrasonic welding of the bump or beam lead to the substrate metal.

Table 10 shows a comparison between the important characteristics of various die bonding methods. It is seen that most of the schemes utilize heavy metals, such as gold, on the substrate making them unsuitable for use in radiation environments. However, two of the systems are suitable because they contain only aluminum on both the chip and the substrate and these are the systems used in the present program. These systems, the Al bump and the Al beam lead system,

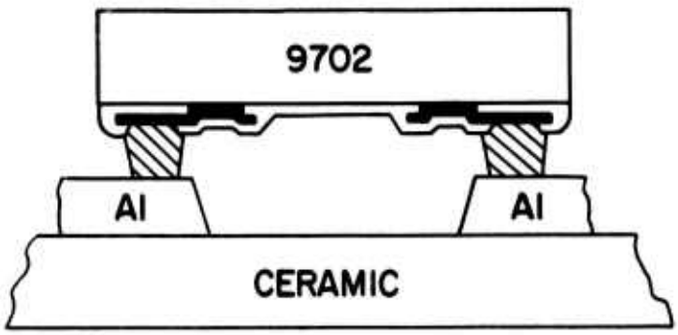


Figure 49 Chip with Al Bumps Ultrasonically Bonded to an Al Metallized Substrate.

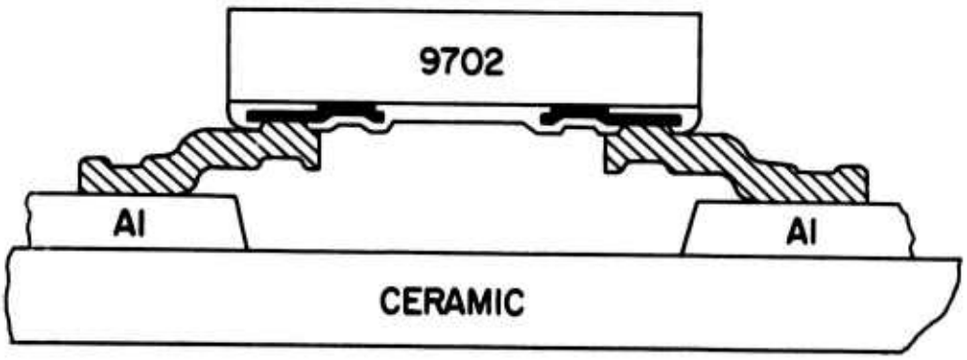


Figure 50 Chip with Al Beam Leads Bonded onto an Al Metallized Substrate.

TABLE 10

CHARACTERISTICS OF LEADLESS DIE ATTACH SYSTEMS

	Ultrasonic		Thermo compression		Solder
	Al-Al Bump	Al-Al Beam	Al-Au Bump	Au-Au Beam	Al-Au Bump
Bump or Beam metal:	0.6 mil Al	2 mil Al	1 mil Al	0.5 mil (Ti/Pt)Au	1 mil Al/Ni/ (Sn/Au)
Substrate metal:	0.6 mil Al	0.4 mil Al	0.1 mil (Mo/Mn)/Au	0.1 mil (Mo/Mn)Au	0.3 mil (Mo/Mn)/Au
Bonding temperature:	25-150°C	25°C	440°C	300-350°C	325°C
Force per bump (4x4 mil) applied on chip	10-30 gr	0	> 100 gr	0	< 5 gr
Tolerable substrate flatness (over the chip dimension)	2-3 μ	10-20 μ	5-10 μ	5-10 μ	5-10 μ
Intermetallic formation	No	No	Yes	No	No
Repairability	Yes	Yes	No	Yes	Yes
Mech. shear strength Per 14 bumps (4 x 4 mil)	> 400 gr	40 gr	> 250 gr	?	500 gr
Heavy metals	No	No	Yes	Yes	Yes
Thermal resistance of contact	~ 8°C wall/bump (.004x.004)	~ 1800°C wall/beam (.003X.002)		~ 1200°C wall/beam (.003X.002)	

have very similar properties, however, the aluminum bump approach results in a superior adherence of the chip to the substrate, and a thermal resistance which is an order of magnitude lower.

Leadless die attach provides only a partial solution to the problem of multiple wire bonds since in present military multichip systems the substrate is attached into a package that still employs wire bonding from substrate to package. The best solution to this problem is to employ a leadless die attach to a substrate which forms part of the final hermetic package and thereby: (a) eliminate all flying wire bonding and (b) eliminate substrate attachment failure which can occur from thermal shock.

A substrate employing aluminum conductors has a number of advantages: It is metallurgically compatible with the chip metallization thereby eliminating undesirable metallic interfaces and intermetallics. The low resistance conductors allow the use of narrow conductor lines that lead to higher circuit density. Good conductor adherence results in good mechanical reliability for chip or package leads which are bonded to the substrate layer. A multilayer metal crossover capability eliminates the use of jumper wires for crossovers on the substrate.

In summary, a multichip system employing leadless die attachment can best be achieved in a radiation-hardened multichip technology by the two approaches just mentioned: (a) flip-chips with aluminum beam leads ultrasonically bonded to aluminum pads, and (b) flip-chips with aluminum bumps which are ultrasonically bonded to aluminum pads. For either system, wafers fabricated with standard processes are used; that is, normal IC's are fabricated using an aluminum interconnection system on the die. The gold beam lead process currently used by most

manufacturers employs a complex metal system composed of Pt or Pd, Ti, Pt, followed by thick Au. Obviously, the IC must be designed for this process. However, any integrated circuit utilizing aluminum metallization can have Al bumps or Al beams applied to it without a complete redesign. This is not true for other multichip assembly methods. In addition, the aluminum to aluminum systems are low Z, fully compatible, with no intermetallics.

DEMONSTRATION VEHICLE

The demonstration vehicle is a six-bit binary full adder as shown in Figure 51. This is a full adder which performs the addition of two six-bit numbers. Sum outputs are provided for each bit and the resultant carry (C6) is obtained from the sixth bit. The intermediate even-numbered carry outputs (C2, C4) are brought out for ease in trouble-shooting during the assembly of the adder. This feature also allows the adder to be used as a 2, 4 or 6-bit adder. The circuit is designed for medium to high speed, multiple-bit, parallel-add/serial-carry applications. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits.

The six-bit adder is fabricated by multichip technology. It contains sixteen dielectrically-isolated radiation-hardened TTL integrated circuit chips which are assembled in a multichip package and interconnected to form the six-bit adder. The integrated-circuit chips are the single-layer anodized aluminum 9702 and 9708 circuits fabricated by the process described in Section IV of this report. These circuits, which are shown in Figure 52 are part of Fairchild's radiation-hardened TTL circuit family. These circuits utilize the following hardening techniques:

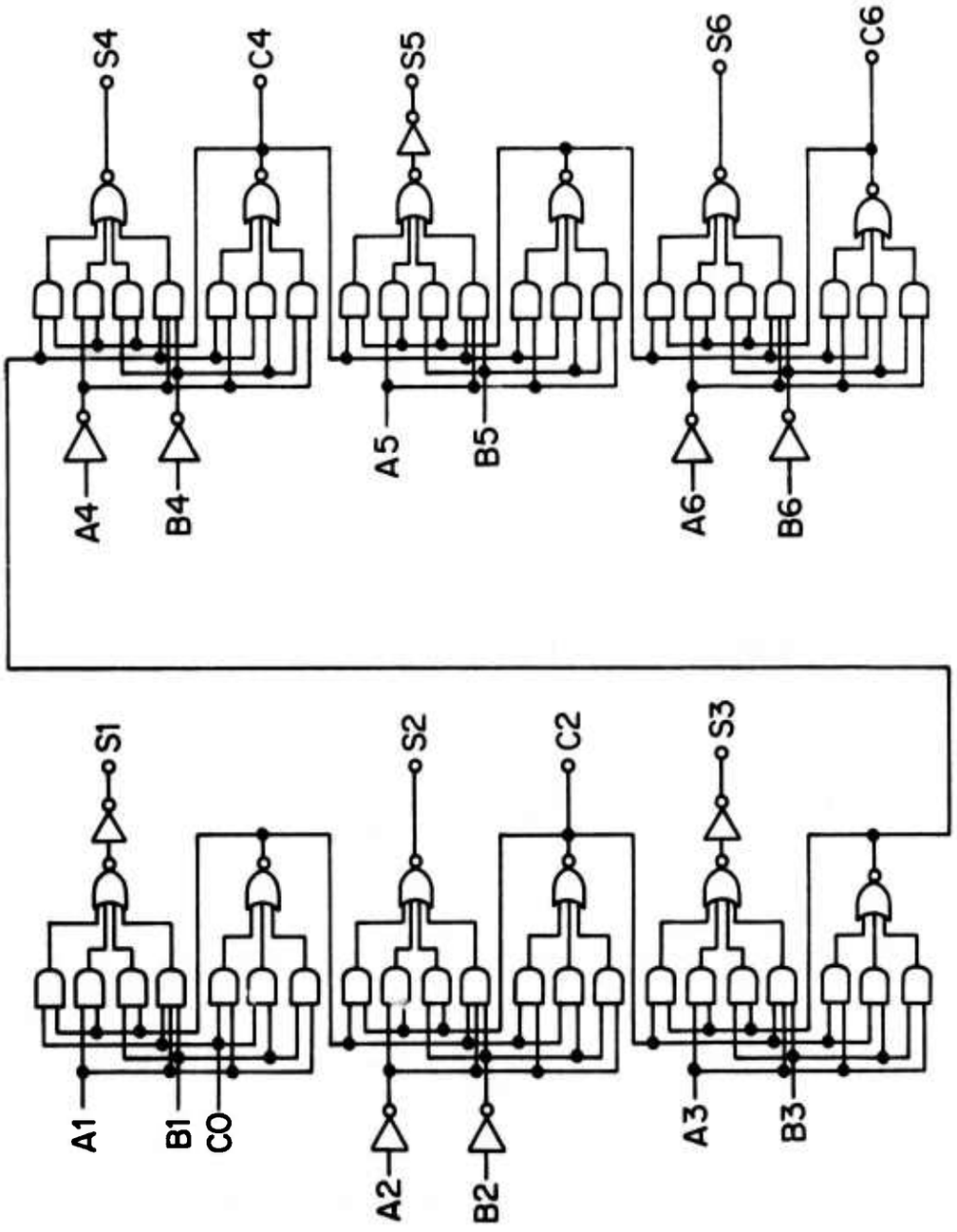
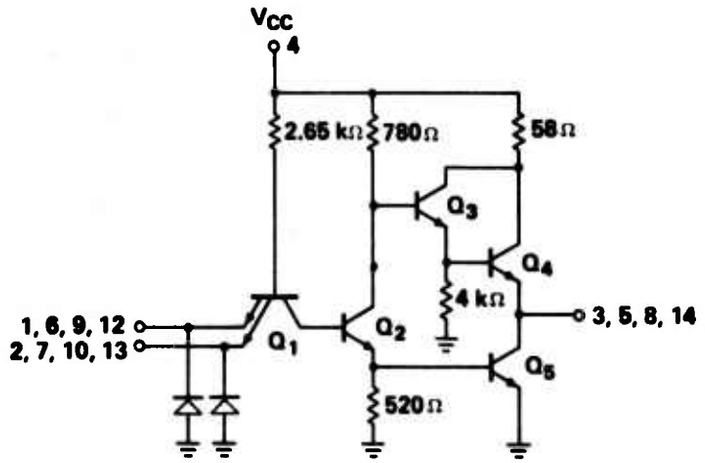


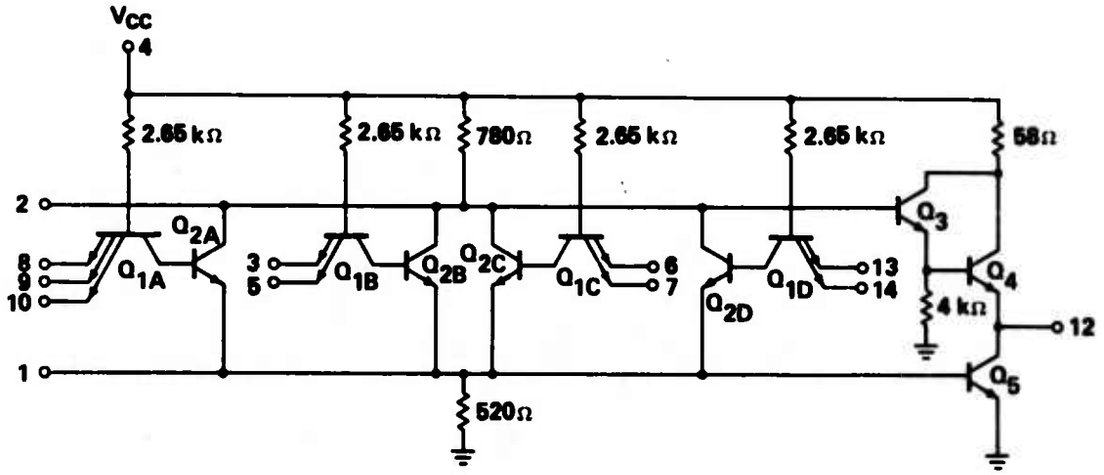
Figure 51 - Functional Block Diagram for Six Bit Binary Full Adder

QUAD, 2 INPUT, NAND GATE
9702/5400



NOTE: CLAMP DIODES ARE OPTION ON INPUTS

SINGLE, 4 WIDE, 3-2-2-2 INPUT, EXPANDABLE A-O-I
9708



NOTE: CLAMP DIODES ARE OPTION ON INPUTS

Figure 52 - Radiation-Hardened TTL Gates

- Dielectric isolation,
- $MoSi_2$ thin-film resistors,
- All-aluminum metallization,
- Thin-film resistor photocurrent limiting,
- Thin-film resistor passivation and scratch protection.

The fabrication process has been modified to provide anodized aluminum interconnections, and aluminum beam leads or aluminum bumps for attaching the chips to a ceramic substrate using flip-chip bonding techniques.

The die sizes of these circuits are as follows:

- 9702----------68.5 x 86 mils
- 9708----------70 x 70 mils

Twelve 9708 A-O-I chips and four 9702 Quad gate chips are used to implement the adder function.

MULTICHIP SUBSTRATE AND PACKAGE DEVELOPMENT

A reliable substrate interconnect system using two levels of metal interconnections was established on a ceramic substrate for the assembly of radiation hardened integrated circuit chips. This substrate allows the bonding of sixteen chips with a chip packing density greater than 20 chips per square inch. The ceramic substrate metallization system and the package were designed to survive a fast neutron flux of 3×10^{14} n/cm^2 and an integrated gamma flux of 10^7 rads. These developments will now be discussed in detail.

Substrate Interconnect System

The substrate layout and the mask set for interconnecting the six-bit binary full adder possess many features heretofore unobtainable. Figures 53a and 53b illustrate the top and bottom layer interconnect metallization patterns. This single substrate interconnect pattern will accommodate flip-chips with both beam leads and bumps. Higher chip packaging densities could have been obtained if only bumped integrated-circuit devices were to be accommodated. Important substrate characteristics are summarized in Table II.

The substrate is considerably larger (2.0 in^2) than the actual substrate area under seal (0.772 in^2) because this was the nearest substrate size for which external connectors and assembly hardware were readily available. A smaller substrate size would have required special drawings, parts, etc., which would have resulted in a considerable increase in the cost of the demonstration vehicle.

The increased costs required to fabricate smaller substrates and assembly hardware were not felt to be warranted for the number of assembled parts which are to be delivered under this contract. Additional key features of this demonstration vehicle are:

- Integrated-circuit chip packaging density in excess of 20 chips per square inch.
- Computer Aided Design (CAD) used for the substrate metallization system and for mask generation.
- Substrate package compatibility with existing Standard Hardware Package (SHP) modules.

Figure 4 shows a cross-section of the six bit adder package and its relationship to edge connectors. This connection system allows

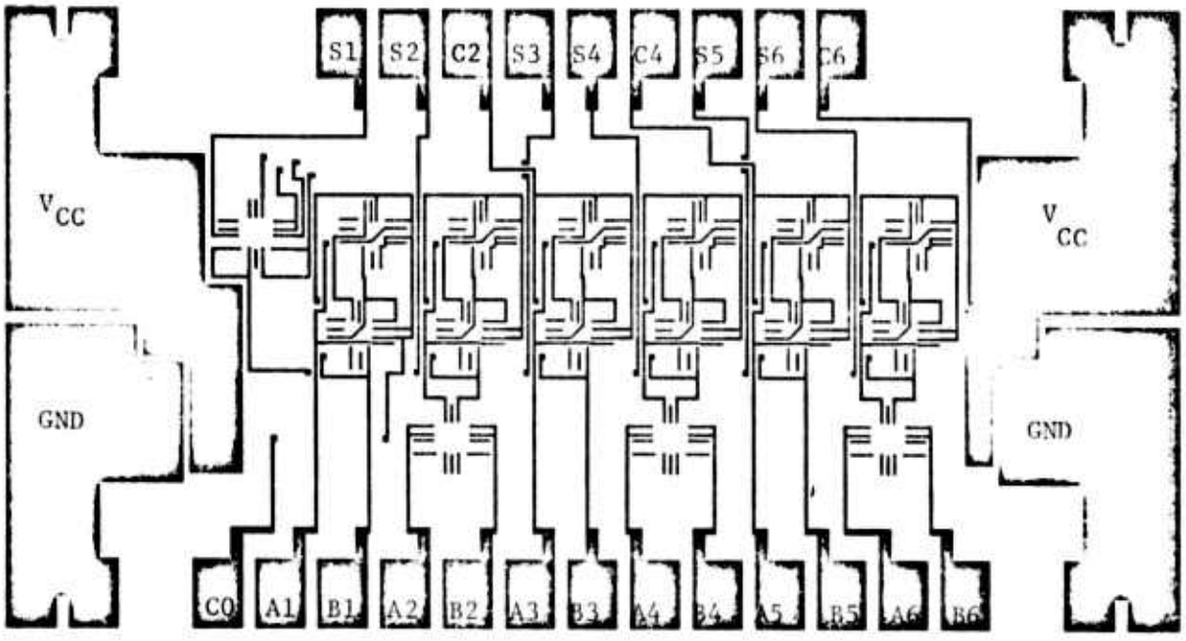


Figure 53a - Six-Bit Binary Full Adder, Bottom Layer Metal Pattern

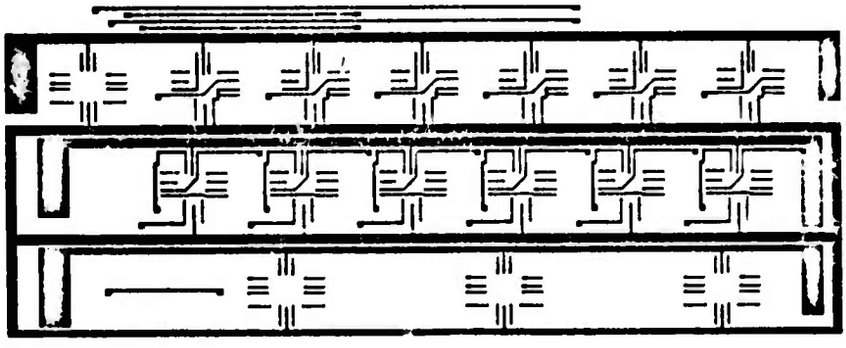


Figure 53b - Six-Bit Binary Full Adder, Top Layer Metal Pattern

Table 11

Substrate Characteristics

CONDUCTORS	
Bottom layer resistivity	3.5×10^{-3} Ω/□
Top layer resistivity	8.5×10^{-4} Ω/□
Line widths: typical	0.005 inches
minimum	0.0035 inches
Line spaces: typical	0.005 inches
minimum	0.0035 inches
DIELECTRIC	
Bulk resistivity	$>10^{14}$ Ω/cm
Breakdown voltage	>200 V/μm
Dielectric constant	∿13
Capacitance	1/8 pF per 5x5 mil crossover
Number of crossovers	199
Number of vias	42
MISCELLANEOUS	
Substrate size	1 x 2 inches
Substrate area under seal	0.772 in^2
Chip Packing Density	20.6 chips/in^2

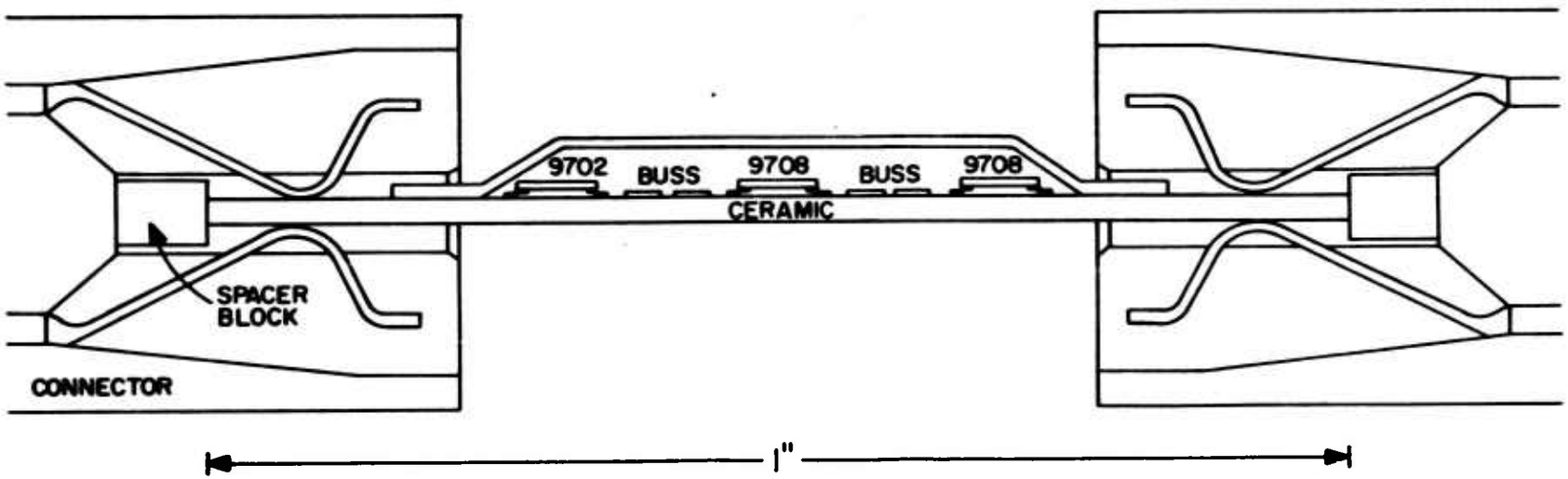


Figure 54 - Package Cross-Section, Six-Bit Binary Full Adder.

easy and convenient addressability of all pads within any testing or operating installation.

Package Sealing

The development of a hermetically sealed package for the 6-bit binary full adder circuit has required the solution of the following production problems:

- Large area sealing cap fabrication
  - (a) Formation of caps with low distortion
  - (b) Flat and uniform cap periphery for sealing
  - (c) Minimizing operator training and sensitivity to cap quality
- Cap metallurgy environmental protection
- Reliable sealing process and jigging
- Evaluation of hermetic seal

The final design of the production tooling and jigging provides a high yield cap fabrication process. The technique contains a minimum amount of operator sensitivity and provides maximum utilization of the Kovar.

The cap is designed to provide the maximum amount of hermetic seal area. The choice of sealants in combination with the long seal length provide the highly reliable hermetic seal. Thermo-cycle testing was used to evaluate the seal hermeticity with excellent results. The hermetic seal characteristics are outlined in Table 12.

TABLE 12

HERMETIC SEAL CHARACTERISTICS

Ceramic Substrate	1.0 x 2.0 inches
Cap Dimensions	1.5 x 0.7 inches
Hermetic seal dimensions	1.35 x 0.55 inches
area	0.742 inches ^{2}
length	3.8 inches
Sealant material	Castorez 154
width	0.050 inches
thickness	0.002 inches
Hermeticity zero hours	1.2×10^{-7}
after 50 thermocycles Of $-65^{o}C$ to $150^{o}C$	4.8×10^{-7}

FABRICATION PROCESSES

Substrate Interconnect Fabrication

The substrate electrical interconnect system is formed by standard integrated circuit processes which result in high yield, good quality substrates. A finished substrate is shown in Figure 55. Basically, aluminum is deposited on the clean substrate surface. The first metal pattern is then defined by standard photoresist masking and etching processes. In order to obtain good pattern delineation the ceramic substrate must meet certain minimum requirements. Such substrates are available from commercial sources of Al_2O_3 ceramics. First layer metal is followed by a glass insulating layer formed by a sedimentation process and subjected to a low temperature densification. Via openings to the first layer metal pattern are formed, again using standard masking and etching processes. The second layer metal is then deposited and defined in the same manner as the first layer metal.

The quality of the interconnects produced is monitored optically at each fabrication step. The specific dimensions used are given in Table 11.

Aluminum Bump and Beam Lead Fabrication

Requirements: Any existing integrated circuit can be prepared for multichip assembly as long as certain requirements are met with respect to bonding pad spacing and relative placement from die to die.

The aluminum bumps are erected directly over the standard wire bonding pads. This requires no special redesign of masks or modifications to standard in-production devices, such as the 9702 and

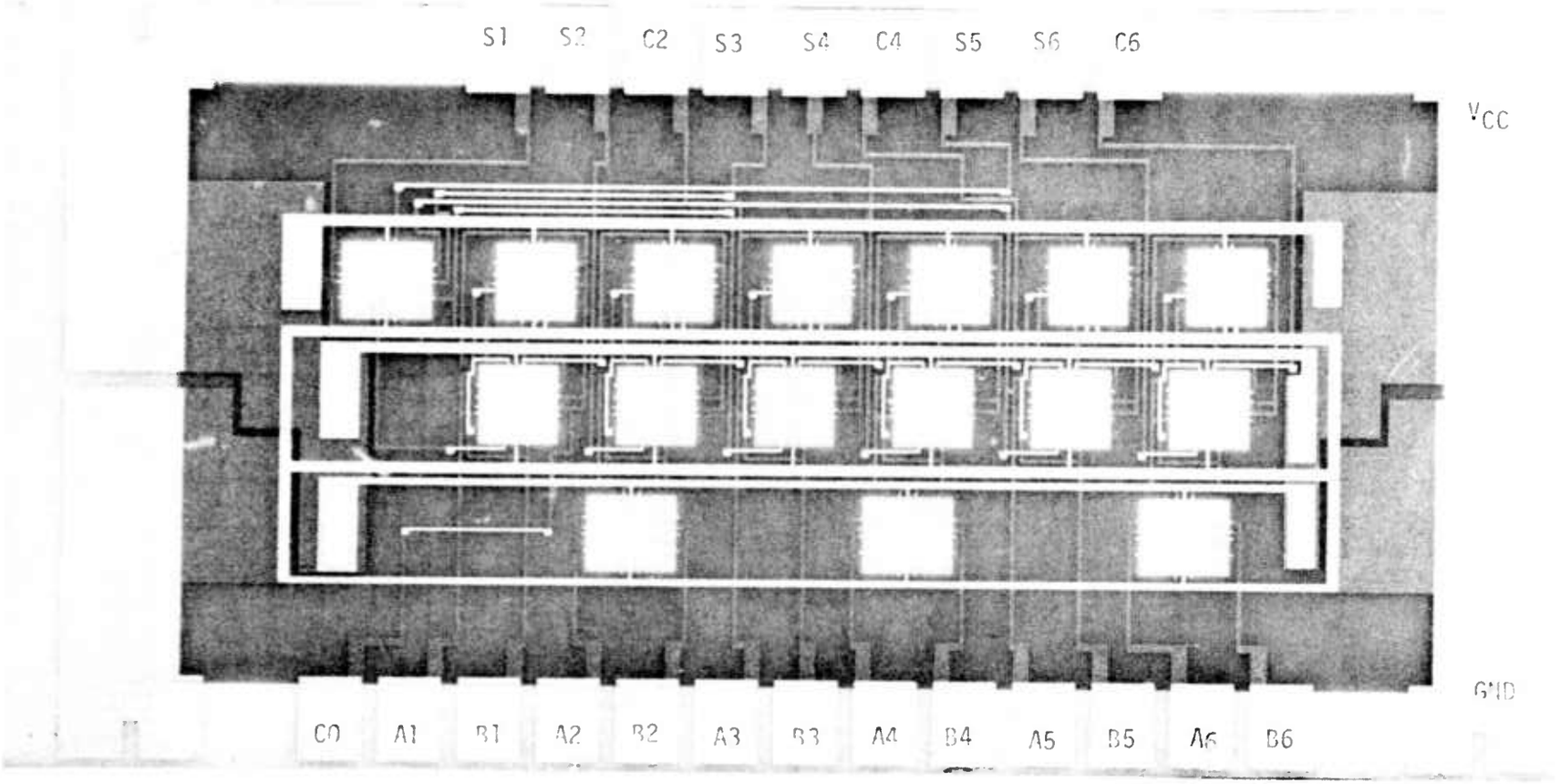


Figure 55 - Ceramic Substrate With Dual Layer Metallization

9708 radiation-hardened TTL gates. However, the general requirement that must be met for a bump 1 mil high and 5 mils square at the base is a bump-to-bump spacing of 2 mils for bonding purposes, i.e., to account for misregistration, sideways slide of the die, etc.

The requirement for beam leads are more stringent because the beams must overlap the next die. Therefore the bonding pads must be interdigitated on opposite sides of dice such that the beams on adjacent dice will be interleaved. In this case the pad to pad spacing should be equal to or greater than twice the beam width.

Since the 9702 and 9708 gate circuit die were not originally designed for beam lead applications, new layouts and masks would have been necessary to meet these beam lead requirements. The costs required for a complete re-layout were not felt to be warranted by the number of assembled parts which were to be delivered under this contract. In order to obtain the silicon area required for beam lead overlap on adjacent die, the beam-lead Vapox and metal masks were stepped in alternate rows and columns to produce the checkerboard pattern shown in Figure 56. This technique automatically reduces the available dice per wafer by one half.

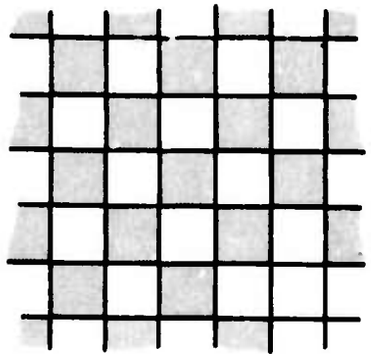


Figure 56 - Stepping Pattern Used to Fabricate Beam-Leads on 9702 and 9708 Circuit Wafers.

No special process requirements are necessary to manufacture aluminum beam leads or bumps. All the processes which are used are standard processes used in semiconductor device fabrication.

Process: The aluminum beam lead and bump process flow is given in Table 13. Basically the two processes differ at only two points. The beam lead process requires a photoresist application to prevent adherence of the beams to the wafer and the bump process requires an aluminum deposition on the backside of the wafer for bonding purposes.

In order to utilize wafers containing 9702 and 9708 gate circuits which were fabricated according to the anodization process given in Table 8 (Section IV), a PVx deposition step is inserted after porous anodization. This layer is included to protect the porous anodic oxide during the delineation of the bump metal. It is not necessary for the beam lead process, but it is used anyway to minimize process variations. Inadvertently, a fairly large number of wafers were processed through bumps without this PVx layer. On these wafers it was found that the bumps were satisfactorily etched without excessive attack to the underlying porous oxide. It is therefore concluded that it is possible to form aluminum bumps directly on the anodized wafer; however, a much lesser degree of process control is required if the anodic oxide is protected by a layer of PVx. Circuits processed by standard production manufacturing methods (not anodized) normally receive a PVx covering in the fabrication process and are therefore suitable for aluminum bump and beam lead fabrication.

Table 13

Aluminum Bump and Beam Lead Process Flow For Anodized 9702 and 9708 Gate Circuits.

Process Begins After Porous Anodization (Step 8, Table 8, Section IV)
Deposit PVx Layer (0.3 to 0.5μm)
Open Contact Pads in PVx (Step #9, Table 8)

BUMP PROCESS	BEAM LEAD PROCESS
Deposit Aluminum (≈25μm)	Photoresist Application
Define Bumps	Deposit Aluminum (≈25μm)
Deposit Al on Backside (≈5μm)	Define Beam Leads
Define Backside Al	Remove Photoresist

Aluminum Alloy (Step #10, Table 4-1)

Electrical Test and Sort

Scribe

Separate Dice

After the PVx deposition the bonding pads are opened and the aluminum is alloyed with the standard processes described in Table 8. At this point, the wafers are committed to either the aluminum bump or beam lead metallization process.

The wafers to be processed for aluminum bumps proceed directly to aluminum evaporation. The aluminum is 25μm thick and is deposited by electron beam evaporation. Photoresist is then applied, exposed (using the bump mask) and developed so that it protects the aluminum in the bump areas. The unwanted aluminum is etched away, the photoresist covering the bumps is removed leaving completed aluminum bumps. The wafers also receive an aluminum deposition on the back of the wafer. The wafers are then ready for electrical testing and scribing into separate chips. A cross-section of the bumped chip is shown in Figure 57 and photographs of 9702 and 9708 die with aluminum bumps are shown in Figure 58. The bump process was found to be reproducible and high yield process.

The wafers to be processed for aluminum beam leads are first subjected to a photoresist process before proceeding to aluminum evaporation. In this process the photoresist is exposed and developed so that it covers all of the wafer surface except for the exposed aluminum in the bonding pads (every other die). Aluminum is then evaporated and the beams are delineated using the same methods that were used for the bumps. The aluminum beam leads are 1 mil thick, about 4 mils wide, and extend over the scribe line onto the adjacent die. The previously applied photoresist is now selectively removed from the wafer surface and from the space between the beam lead and the wafer surface. The resulting structure consists of aluminum beam leads anchored only at the bonding pads. Figure 59 is the photograph of 9702 and 9708 wafers with beam leads.

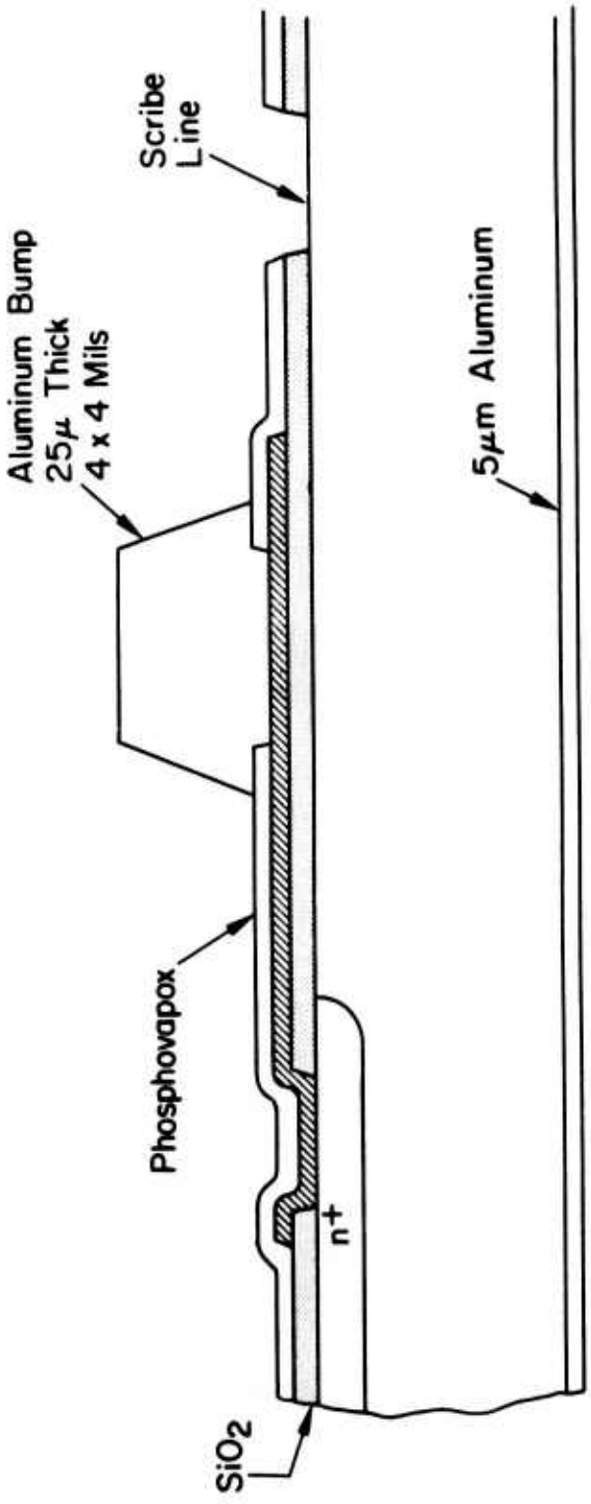
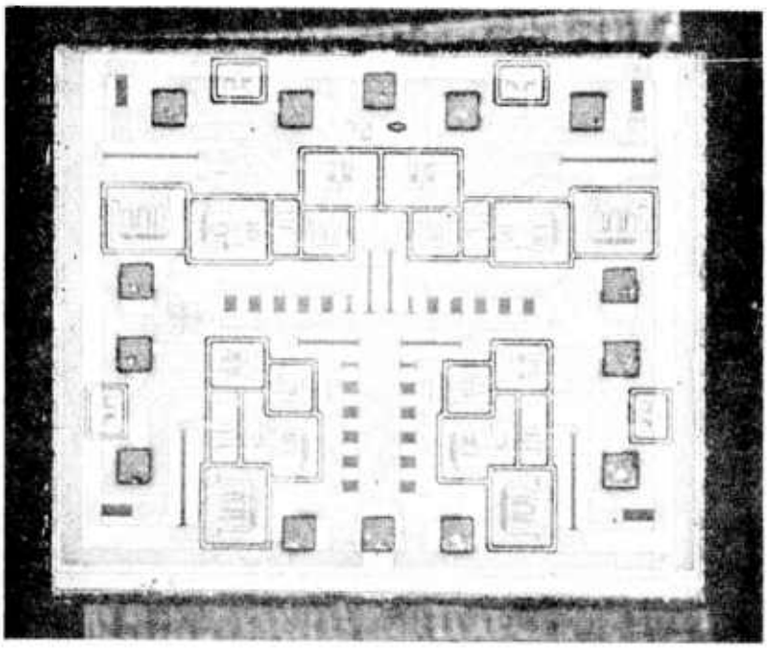
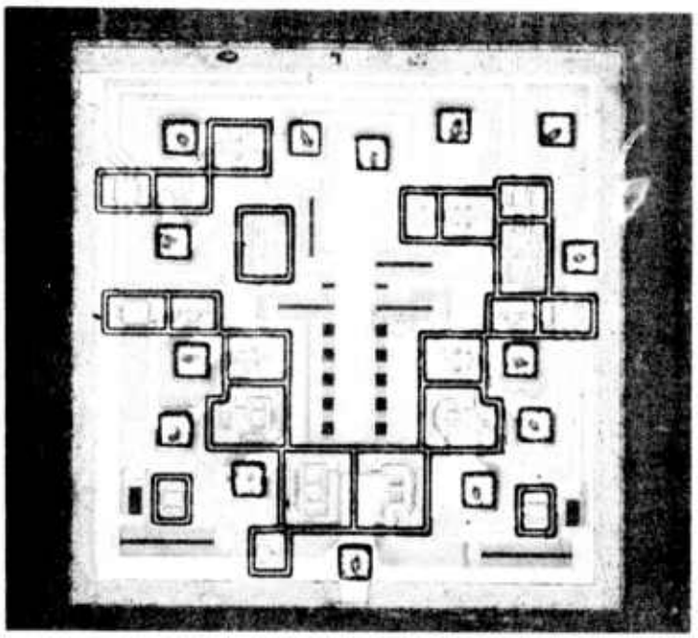


Figure 57 - Schematic Cross-Section of an Aluminum Bump

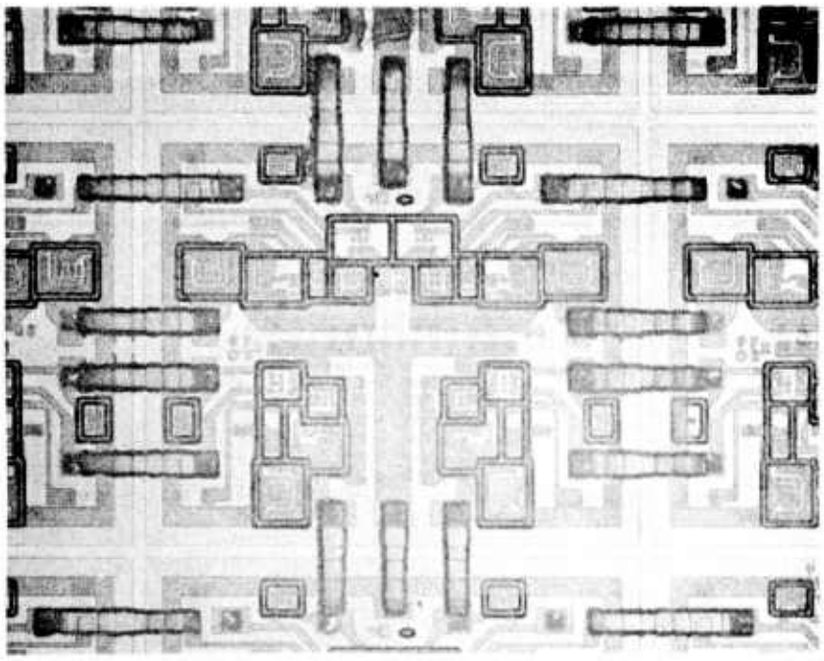


9702

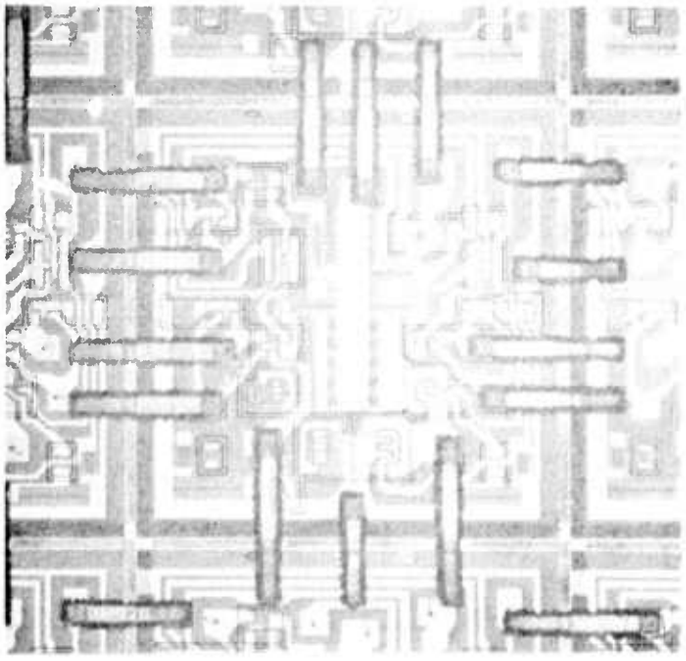


9708

Figure 58 - Photo of 9702 and 9708 Circuit Chips with Aluminum Bumps.



9702



9708

Figure 59 - Photo of 9702 and 9708 Circuit Wafers with Aluminum Beam Leads. Note the Extent of Beam Overlap on Adjacent Dice.

PROCESSING DIFFICULTIES

Beam Leads

Substantial yield losses were incurred during the production of both diced 9702 and diced 9708 circuits having aluminum beam leads. The most significant processing problems are the following:

On-Wafer Losses

(1) Statistically, 50% of the electrically acceptable dice are lost to the "checkerboard" matrix; this pattern was necessary insofar as the original bonding-pad placement on adjacent dice was not designed for a beam-lead configuration.

(2) When the thick (3.0 μm) 200 cs photoresist is applied prior to beam-aluminum evaporation an accumulation of the photoresist in scribe-line areas can cause a "wrinkling" in the beam metal where it crosses the scribe line. Upon defining the beams, metal etchant is evidently able to attack the beam underside in scribe-line areas as shown in Figure 60. This problem can be reduced but not eliminated through adjustment and repetition of the photoresist processing.

(3) During the beam-aluminum evaporation (15 to 20 minutes), significant energy is supplied to the substrate which although not intentionally heated can achieve temperatures in excess of 200°C in the deposition. These temperatures cause undesirable chemical-bond linkages within the photoresist underlying the beam metal such that its removal after beam definition becomes extremely difficult. Extensive solvent cleaning causes many beams to fail at the beam-bonding-pad interface which has poor mechanical integrity having been formed at relatively low temperatures. An alloying operation following these cleanings improves the mechanical strength of the remaining beams.

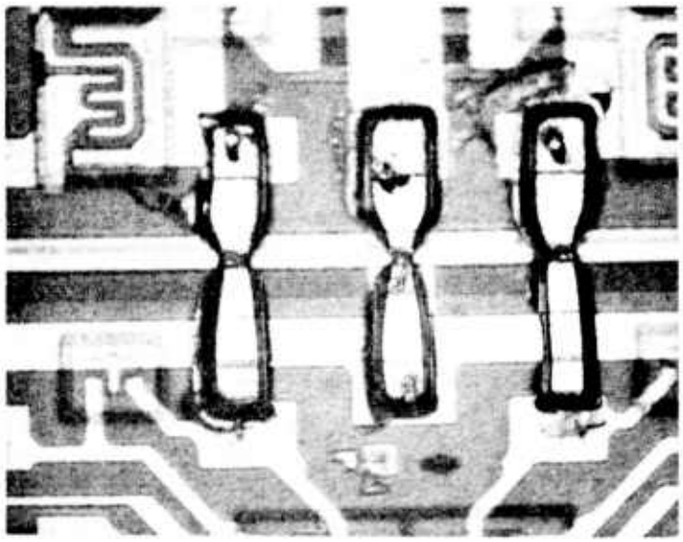


Figure 60 - Beam-lead failure caused by etched underside in scribeline area.

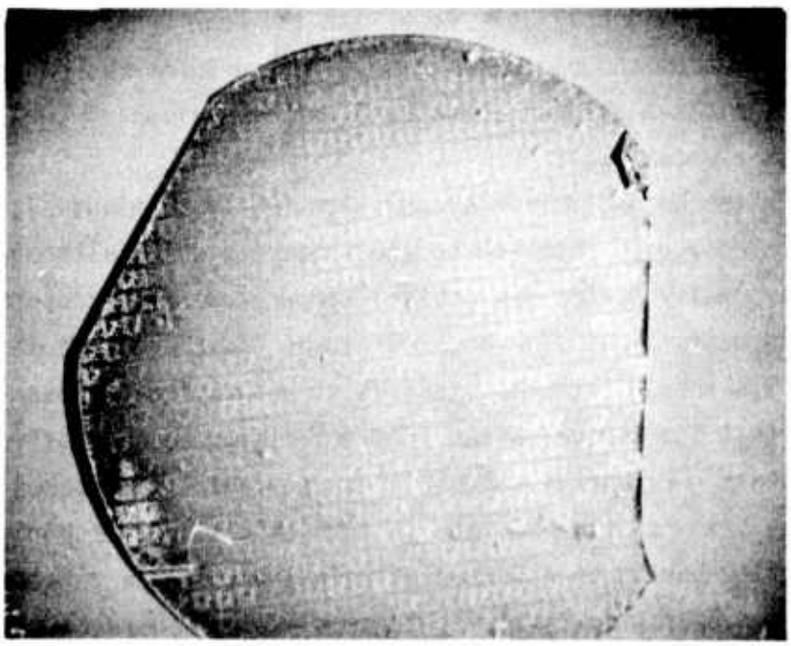


Figure 61 - Blistering and lifting of beam-lead aluminum evaporated onto thick photoresist.

(4) Another problem associated with heating during beam-metal evaporation is an occasional blistering and separation of the beam metal as shown in Figure 61 these losses are comparable in extent to those in item (2).

(5) During beam definition, insufficient aluminum etching causes substantial "bridging" between beams (shown in Fig. 62) while over-etching causes a "clearing" of the original bonding-pad metal (shown in Fig 63; if not catastrophic, this reduction in conductor cross-section creates severe reliability problems. To control the metal etching and compensate for on-wafer thickness variations in beam metal, each wafer must be etched individually; under these conditions, both insufficient and excessive etching commonly occur on the same wafer. The over-etch problem could be corrected by redesigning the beam-metal mask such that the etched-back portion of the beam remains well away from the bonding-pad borders; however, this would involve considerable time and expense.

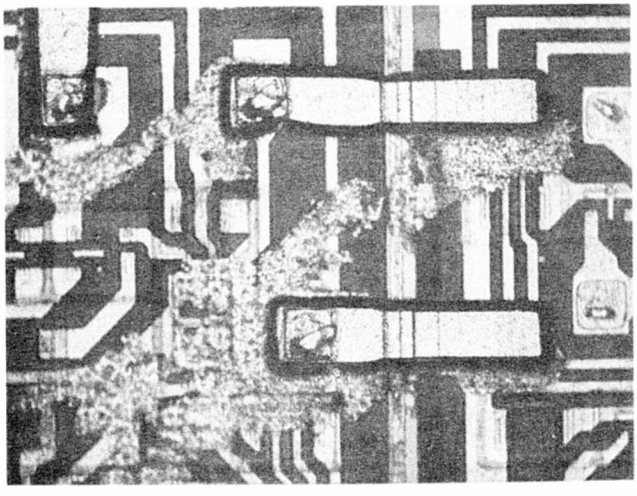


Figure 62 - Aluminum bridging between aluminum beam leads.

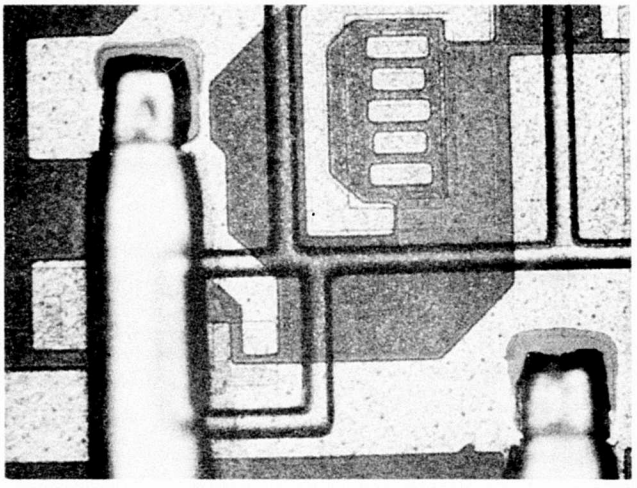


Figure 63 - Over-etched aluminum beam and associated "clearing" of original bonding-pad metal.

(6) Yield losses after beam definition become extremely sensitive to handling; the two most common beam failures are of the "interfacial" and "tearing" types shown in Figures 64 and 65 respectively.

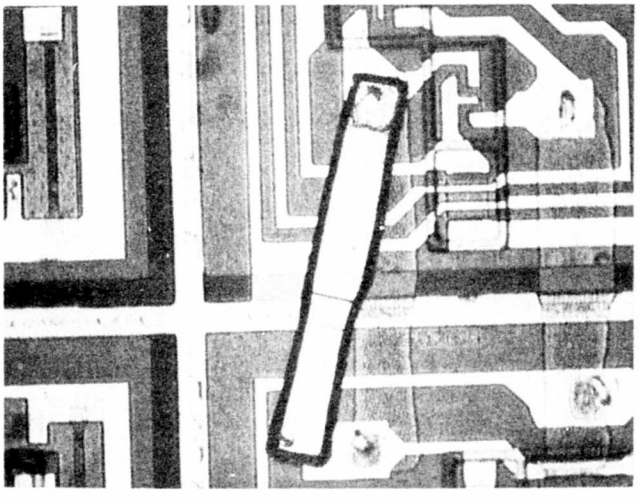


Figure 64 - Aluminum-Beam failures occuring at the beam-bonding pad interface.

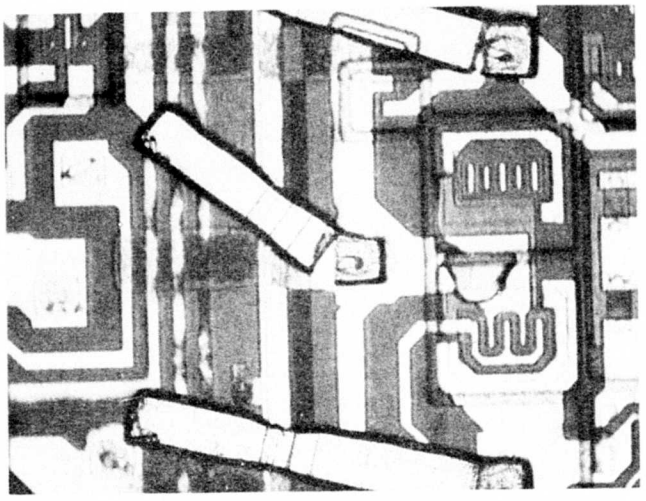


Figure 65 Aluminum-beam "tearing" failure.

The beam-bonding-pad interface problem is that described in item (3) and can be greatly improved by subsequent high-temperature (530°C) heat treatments. However, these temperatures affect any residual photoresist beneath the beam metal causing adherence of the beam to the wafer surface which results in either beam failure or distortion during the dicing operation.

(7) Mechanically probing (wafer sort) the beam leads after the 530°C heat treatment can cause both tearing and interfacial failures. Well-placed probes, extreme care during the probe sequence, and probing each wafer in two separate passes (to ensure probe-beam contact only on potentially good dice, i.e., every other die) minimize but do not eliminate this yield-loss mechanism.

Die and Dicing Losses

(8) After backlap-thinning the wafers, a scribe-line mask is mounted with paraffin on the "front" (circuit) side of the wafer to facilitate "backside" diamond scribing. Although liquified wax is used in this step, a significant number of beam losses is incurred at this step.

(9) Once scribed, the wafers are diced by placing them on a hard-rubber pad and gently pressing down on them with a rubber roller; any adhesion between the beams and wafer surface (possibly enhanced as described in item (6) causes an extreme number of beam failures and distortion even with the most careful handling. Figure 66 shows a typical example of a beam distorted through handling.

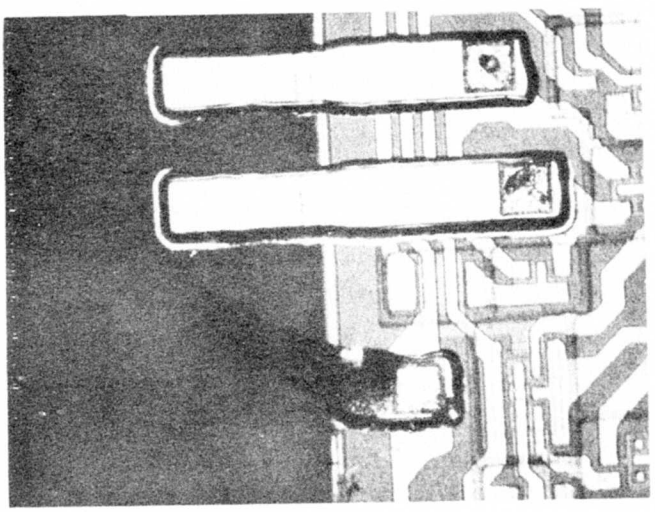


Figure 66 - Aluminum beam distorted through handling.

(10) After dicing, physically separating electrically good and bad dice from one another and placing them into cavity plates (using small vacuum wands) causes additional beam failures and/or distortions. Other methods of die storage were attempted but either proved unrealistic or provided little yield improvement.

In addition to the enormous losses by the above mechanisms, the metallurgy of the aluminum beams is such that they are mechanically brittle; that is, once deformed they tear or fracture very easily during attempts at straightening. This property in combination with exceedingly low yields prior to assembly (for which the equipment and techniques

had not been developed) rendered the beam-lead version of the 6-Bit Adder not realistically manufacturable.

"Bumped" Dice

Often, when a die was removed from the ceramic substrate (because of electrical failure after assembly or mechanical failure during shear testing) one or more of the aluminum bumps would shear in a plane parallel to the ceramic and in the approximate center of the bump metal. This failure was extremely costly in that part of the bump remained on the die and part on the ceramic precluding repairability and causing the loss of both the ceramic and all dice previously assembled onto that ceramic. This problem was particularly acute in the case of 9702 dice and was evidently the result of depositing the bump aluminum in two separate evaporation sequences. Therefore, to provide new dice for assembly, additional wafers of the 9702 circuit were needed on which the thick bump metallization was deposited all in a single pump-down in a large-capacity evaporator.

In addition to the bump-shearing problem, an assembly difficulty arises from "parapets" or ridges around the bump surface to be bonded. The ridge (shown in Figure 67) is an extension of the original surface topography and creates a mechanical reliability problem by reducing (in many cases) the total area of contact between the bump and the ceramic metallization.

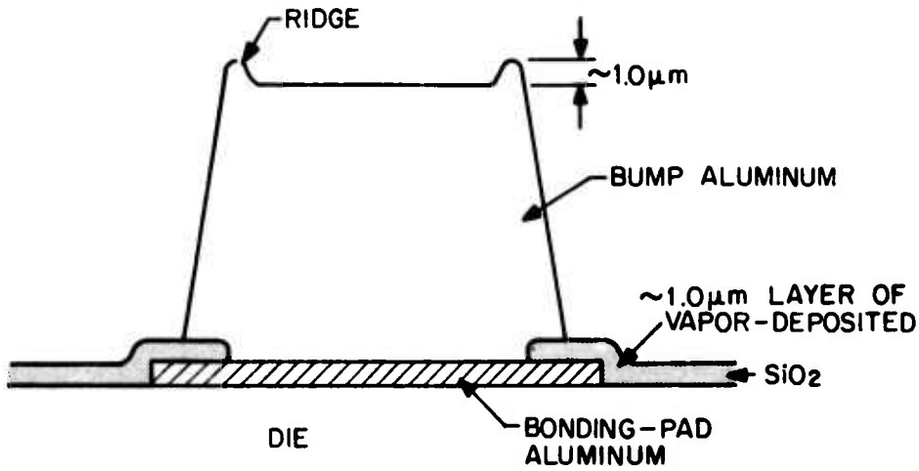


Figure 67 - Cross-section of an aluminum bump and underlying die surface.

This problem was reduced but not eliminated by adjusting photo-masking and etching during bump definition and by optimizing bonding parameters.

ASSEMBLY AND ELECTRICAL TEST

Bond Evaluation

Assuming that all bumps on a die share the same appearance after bonding (which assumes well controlled mechanical dimensions), there are certain visual clues to the effectiveness of the bump-to-substrate metal bond; Figure 68 shows some critical criteria. A "good" appearance after die removal is evidence of both mechanically and electrically effective bonding. Shear-strength performance of an acceptably-bonded 9708 circuit will exceed 400 grams if these criteria are met. Figures 69 and 70 are photomicrographs of a "good" bond (shear strength >1000 gm) showing the bump and substrate metal, respectively. The shear forces are applied perpendicular to the direction of ultrasonic agitation; note the perpendicular striations in Figures 69 and 70 ; these are another indication of good bonding. In contrast, Figures 71 and 72 are photomicrographs of a poorly bonded bump and associated substrate metal; note the difference between these figures and Figures 69 and 70 .

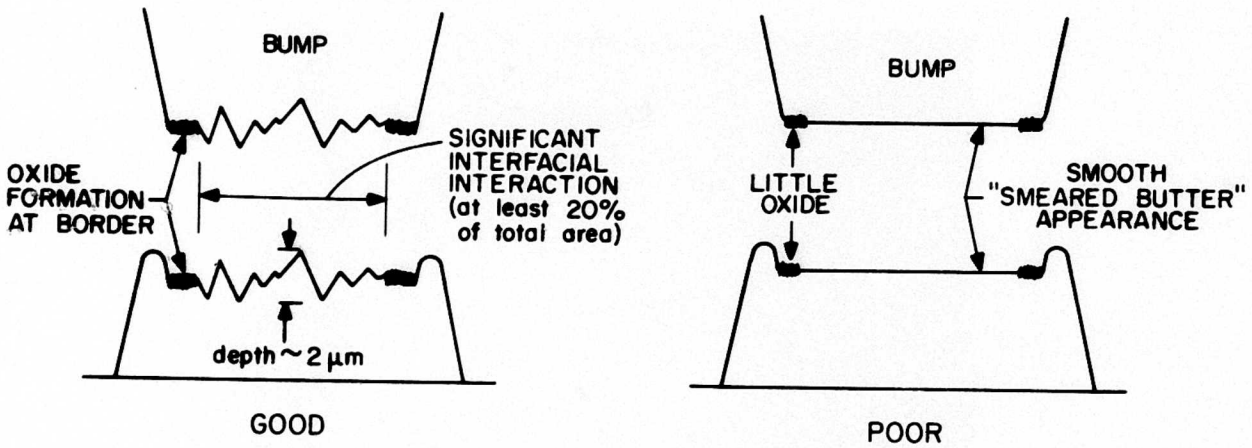


Figure 68 - Bond features after die removal.

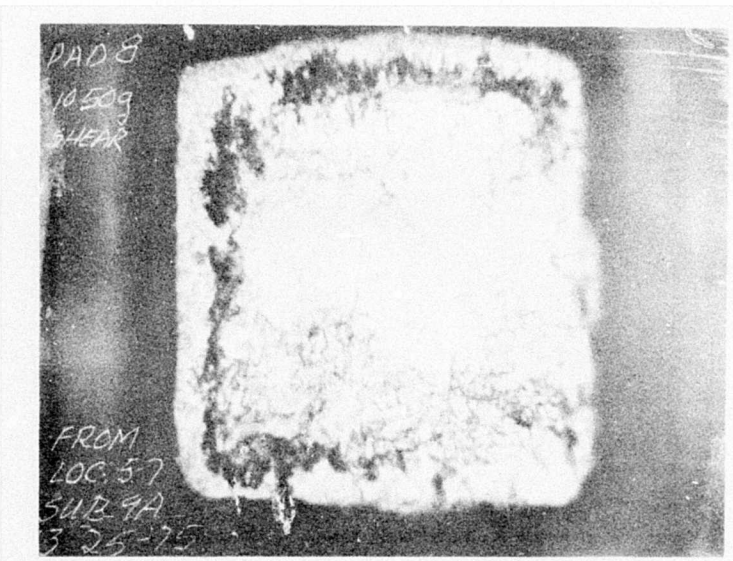


Figure 69 Sheared Bump with Acceptable Appearance.

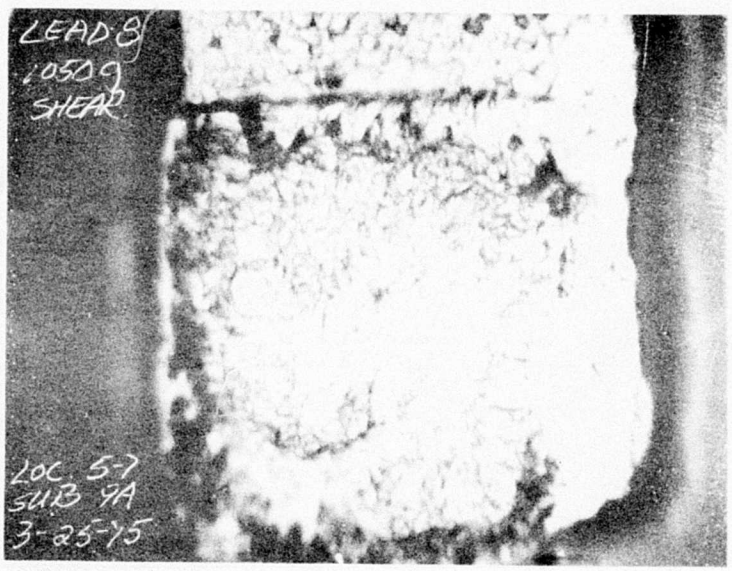


Figure 70 - Substrate metal beneath aluminum bump of Figure 69 .

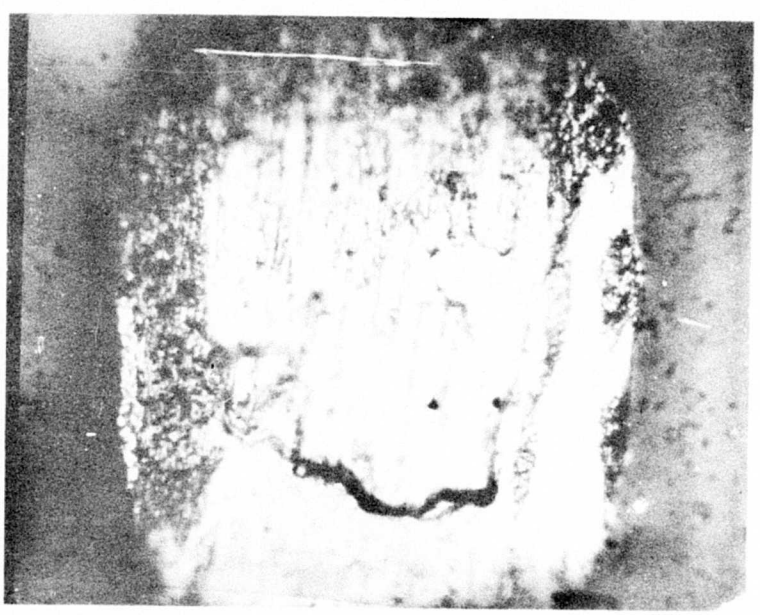


Figure 71 - Sheared Bump With Unacceptable Appearance

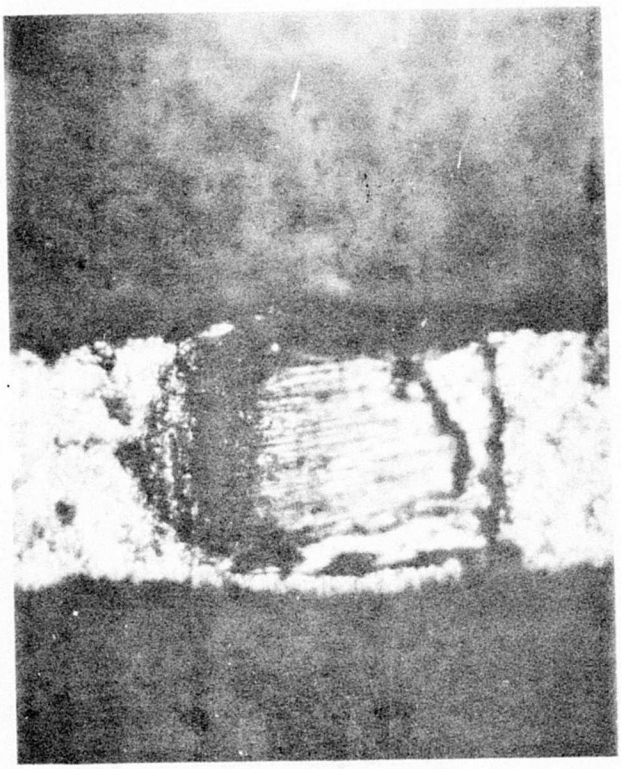


Figure 72 - Substrate metal beneath aluminum bump of Figure 71 .

Better bonds could have been achieved if both bump and substrate metal had been deposited under the same conditions assuring similar grain structure and hardness; this was not the case. In addition, better bonds are possible with larger substrate-metal runs; Figure 73 shows two different bump-substrate-metal configurations. Past experience with similar bonding on other devices indicates that the improved configuration (when space permits) offers at least 3 significant advantages: (1) Improved bond shear strength (approximately 700 grams versus 500 grams for our dimensions), (2) considerably easier chip-to-substrate alignment and (3) improved adhesion properties at the metal-run-ceramic interface.

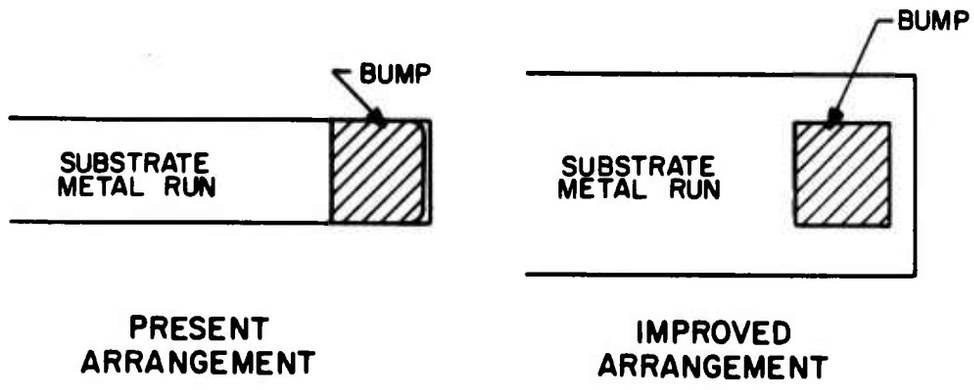


Figure 73 - Configuration of bump and substrate metal.

Substrate Cleaning

Experiments were performed to determine the suitability of different cleaning procedures for the ceramic planes (and associated metallization) prior to ultrasonic bonding. The cleaning procedures were evaluated terms of chemical reactivity with the metal runs and subsequent bond strength, appearance and reliability. Three procedures were evaluated: (1) Cleaning in a cold (25°C) aluminum etchant, (2) cleaning in 100:1 H_2O-HF solution and (3) cleaning in a hot (80°C) aluminum etchant. Based on this evaluation, our present pre-clean involves a 30 second dip in room temperature 100:1 HF in deionized water followed by a thorough water rinse and drying in a stream of dry nitrogen.

After beam lead or bump fabrication, the wafers are electrically tested to determine the parametrically good circuits. The rejected circuits are marked so that they may be eliminated after wafer scribing. Few special wafer probing methods are required and the wafer probe set-up used is essentially the same as that employed to test standard wafers without beam lead or bump interconnects.

After electrical testing the wafers proceed to wafer scribing and die separation. The wafers with bumps require no special precautions. After backlap thinning, the wafers with beam leads must be scribed from the backside of the wafer because the beam leads extend across the scribe line. The actual scribing may be performed with a diamond point or with a laser. After scribing the wafers are broken into chips. The electrically good chips are retained for multichip assembly and the remaining chips are discarded.

Bording

A key factor in obtaining good bonds is the use of a good bonding machine. For leadless die attach with bumps and/or beam leads the bonding machine must perform two basic functions:

- Optically position and align the die with bumps or beam leads to the substrate pads with an accuracy of ±0.5 mil.
- Deliver a controlled amount of energy to the beam or bump interface to make the bond reproducible.

Fairchild has developed a highly effective numerically controlled ultrasonic bump bonder for multichip assembly. The latest model includes unique and improved bonder control, automatic stage movement and pre-positioning, and the capability to conduct electrical testing during assembly. Figure 74 is a block diagram of this bonding and testing system. This system is called the Integrated Multichip Test System or IMATS. Figure 75 is a photograph of the bonding stage of this system.

For the aluminum bump bonding procedure, the bumped die is held by the bonding tool. The die is then automatically aligned by the IMATS and placed face down on the substrate metallization pattern. Ultrasonic energy (for bonding) is coupled from the bonding tool, through the backside aluminum on the bumped die, through the die to the interface between the aluminum bumps and the substrate. As a result all bumps

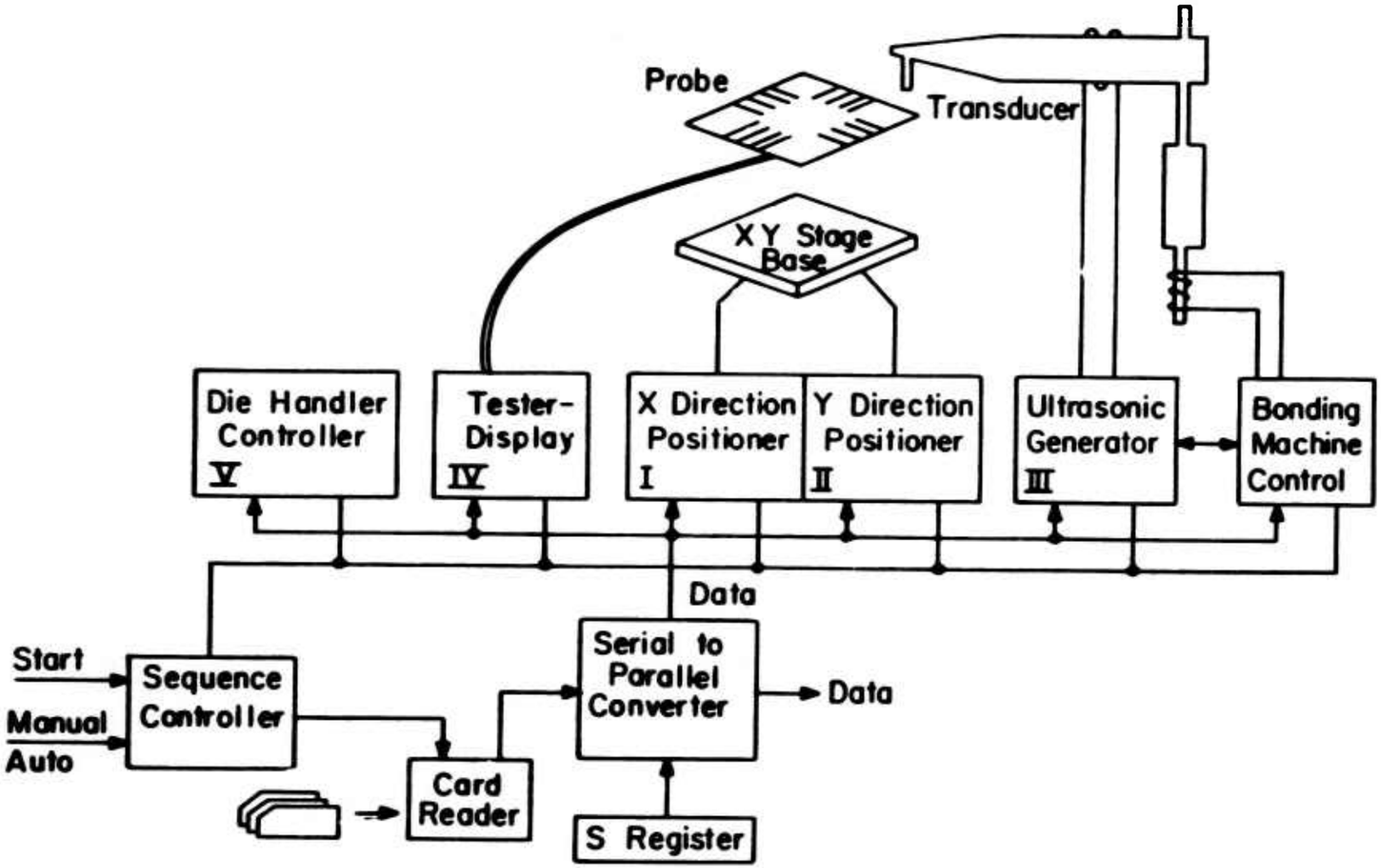


Figure 74 - Integrated Multichip Assembly Test System (IMATS)

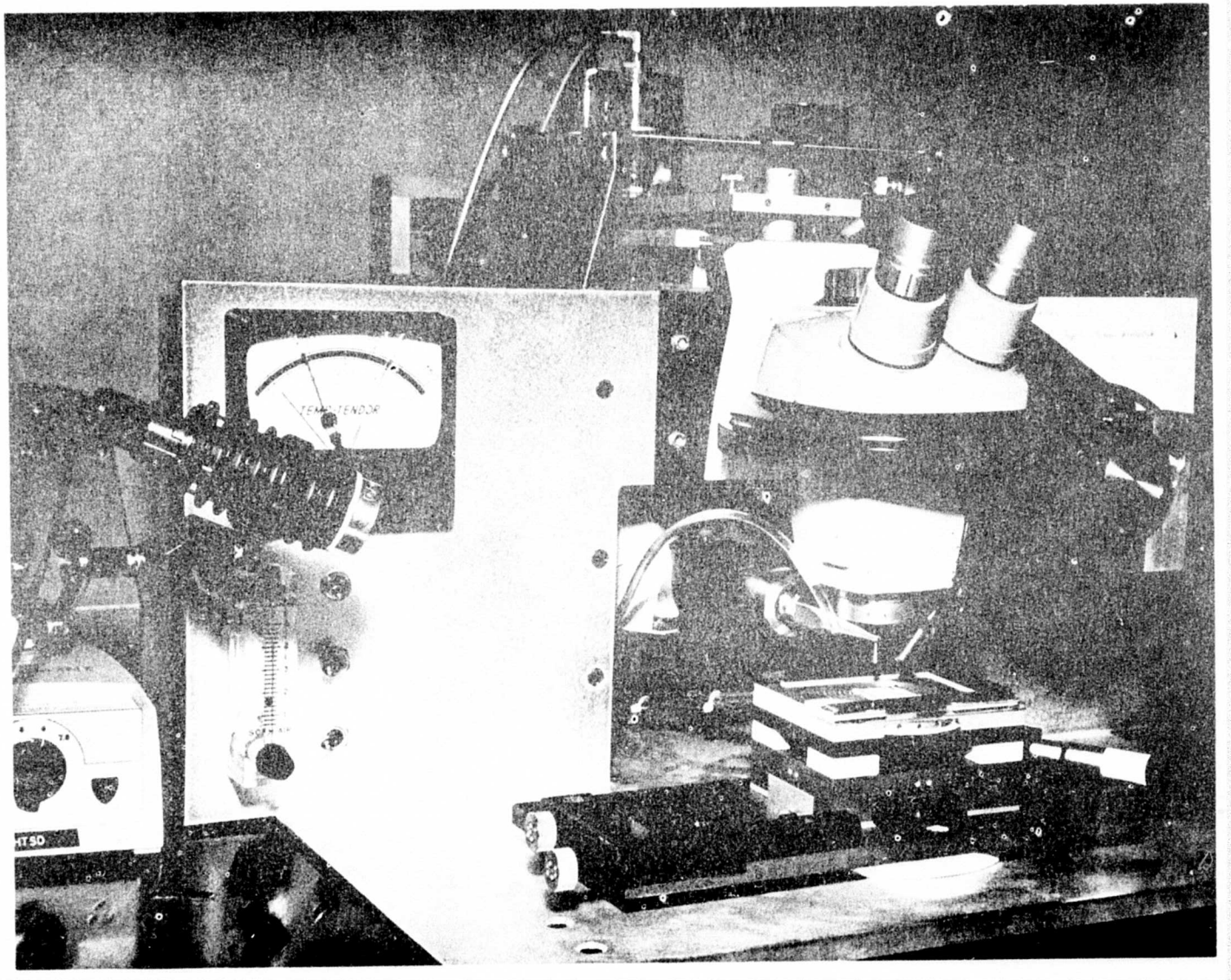


Figure 75 - Aluminum Bump Ultrasonic Bonder - A Part of the IMATS

on the die are bonded simultaneously to the substrate. Once a die is bonded, it is electrically tested to determine if it functions properly. The advantage of this procedure is that if a die with bumps is determined to be electrically defective, then it can be replaced with another. Removal of defective bump dice is accomplished by shearing. After die removal, the substrate is then ready for a second die bond to complete the repair. The removal and repair of beam lead dice is not as straightforward; the die is easily lifted with tweezers but the bond areas must be cleaned of the previously bonded beams before a new die can be attached.

A photograph of a six bit adder multichip assembly using dice with aluminum bumps is shown in Figure 76 a color display of the entire anodization and assembly process was produced and delivered to the Air Force Materials Laboratory per contract requirements. Figure 77 shows a photograph of the completed display.

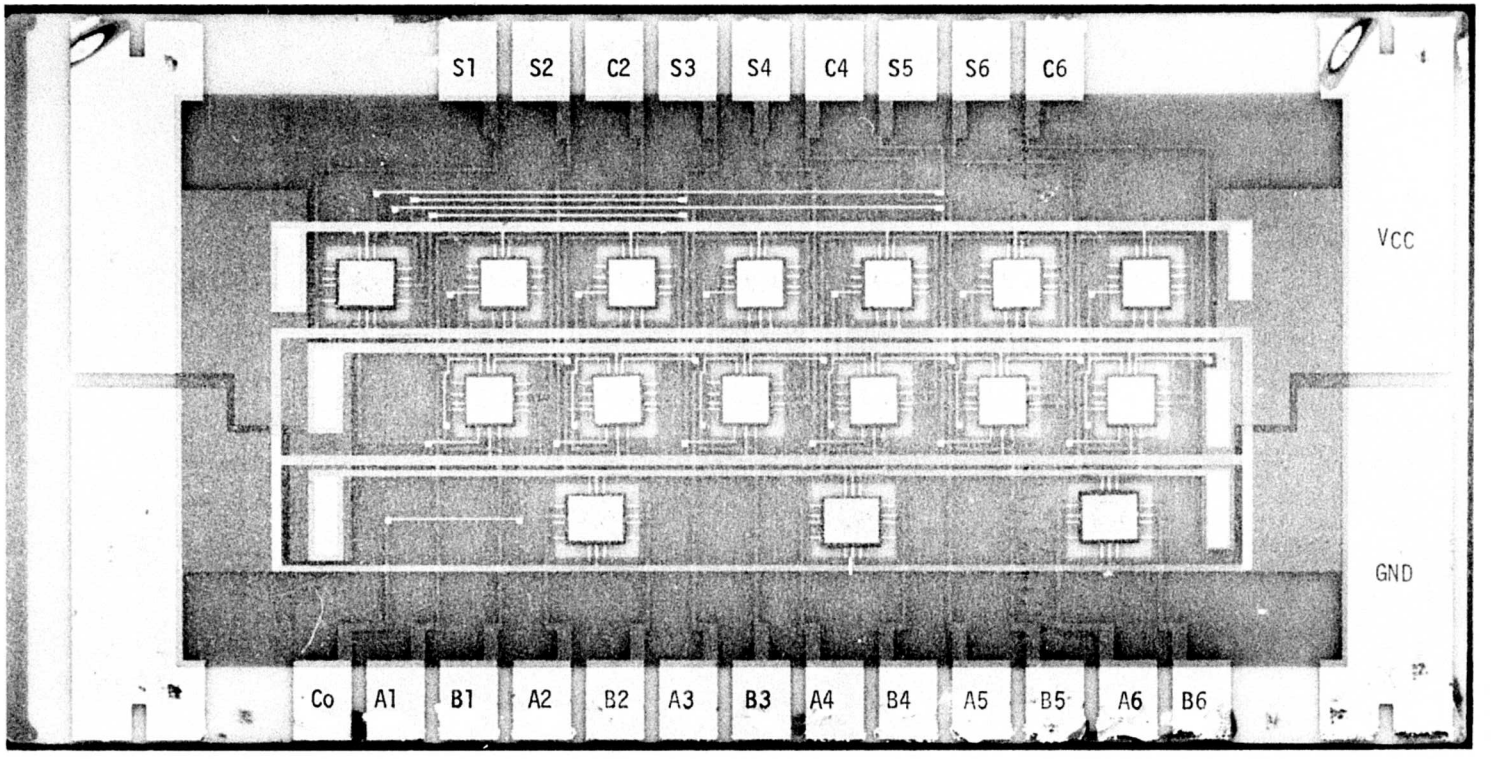


Figure 76 - Completed Assembly For Six-Bit Adder.

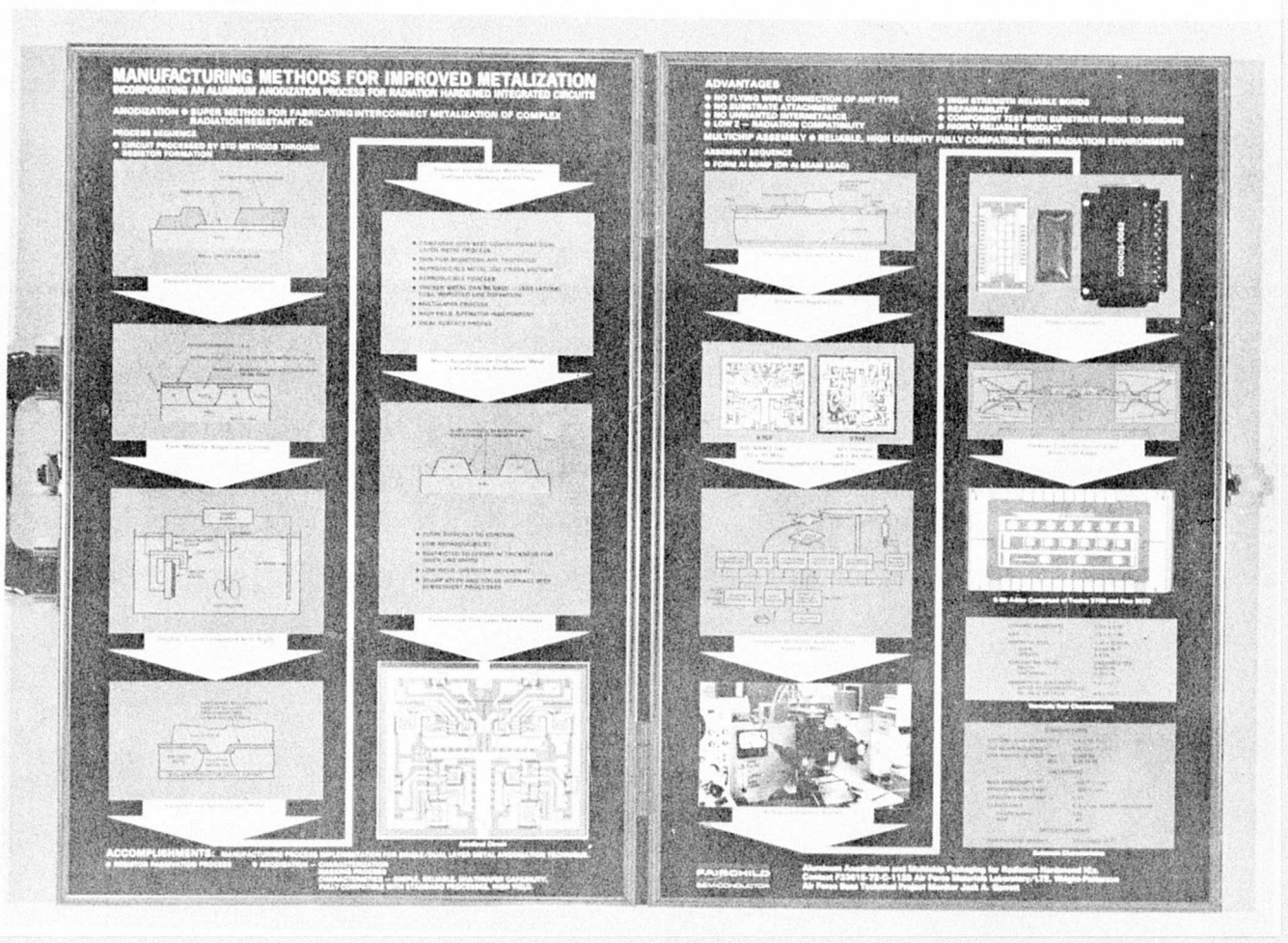


Figure 77. Photograph of the color display showing entire anodization and assembly process for the multichip 6-Bit Adder.

SECTION VI

SUMMARY AND CONCLUSIONS

Manufacturing methods and processes have been developed for the fabrication of single and dual layer metallization utilizing aluminum anodization. These methods and processes were specifically developed for radiation hardened integrated circuits. In addition, multichip assemblies were fabricated using radiation hardened integrated circuit dice with aluminum beam leads or aluminum bumps. These dice were attached to aluminum interconnections on a ceramic substrate which was then assembled in a hermetically-sealed package.

In developing and instituting the anodized aluminum manufacturing process the following tasks were completed:

- The appropriate masks for aluminum anodization of specific integrated circuits were designed and fabricated.
- The effects of aluminum anodization on thin film resistors were studied and a determination of the protection necessary to prevent anodization of the resistors was made.
- Anodization conditions were optimized for aluminum delineation, i.e., evaluations were made of electrolyte composition, the required current density and voltage, and optimum aluminum properties.
- Resist-masking and anodization electrolyte compatibility were evaluated, but this approach is not recommended.
- Compatibility was established between the anodization processes and the assembly processes, i.e., wire bonding, aluminum beam

and bump fabrications.

- Demonstration of the process was carried out by the fabrication of 9702 and 9708 TTL IC gates and 4-bit shift registers using anodized aluminum interconnections.
- An evaluation of the dielectric and electrical characteristics of anodized integrated circuits has been made.
- A multi-wafer anodization process was set up in a manufacturing area.
- The reproducibility of the system was tested and process controls established.
- An evaluation of the reliability of integrated circuits using multilayer anodized aluminum interconnections was completed.
- A simple, effective and reliable multiwafer anodization process has been specified.

Processes and techniques were investigated and established for the assembly of radiation-hardened multichip integrated circuits, for the manufacture of ceramic substrates with multilayer aluminum interconnections, and for the fabrication of aluminum bump and beam lead flip chips and the associated bonding processes. Specifically the following tasks were completed:

- Bump and beam lead masks were designed and fabricated.
- Substrate masks for the demonstration vehicle were designed and fabricated.
- Processes and process controls necessary to achieve good adherence of the substrate metallization were established.

- The compatibility and adaptability of anodization processes and substrate metallization were evaluated and established.
- Processes and controls were established which achieve reproducible flip chip bonds and the AFML was provided with conductivity samples for evaluation of those controls.
- Fabrication of the ceramic substrates necessary for the assembly of the demonstration vehicle - a 16-chip, radiation-resistant, 6-bit binary full adder - was completed.
- A determination was made of those factors affecting quality, yield, and cost of the substrate and methods for controlling those factors were instituted.
- Fabrication and delivery of electrically acceptable units of the 6-bit adder was completed.

- A color display of the entire anodization and assembly process was produced and delivered to AFML.
- Two large-scale hybrid memory planes were delivered to AFML for additional evaluation of the all-aluminum bump die attachment.

Comments About Aluminum-Bump Bonding

This project was worked upon in parallel with a company funded project also exploring Al bump-to-bump technology. Since the development problems for both programs were greater than expected the elapsed time to complete samples was much longer than anticipated. This resulted in both advantages and disadvantages. The development of the company funded project has progressed significantly since the start of this program and more detailed knowledge is now available in understanding the requirements of producing good Al bump bonds.

Production of the wafers for 9702 and 9708 die was stopped after a sufficient number of test wafers were available. In starting the necessary bonding experiments, these wafers had the Al applied in the then available "research" type electron beam evaporator. This evaporator lacked the type of control now available to us in the new planatary

evaporator being used. We are now able to control Al texture and hardness on the wafer so that it matches that on the substrate. This similarity in Al results in more uniform and stronger bonds on all bumps in a die. Unfortunately we were not able to obtain new wafers for 9702 and 9708 die at this late date to provide a better Al match. The Al on 9702's and 9708's is harder and has a finer grain than the Al on the substrate. This results in a deeper melting, during bonding, of the substrate Al and a shallower melt on the bump. The result is less interface attachment and less bond strength than is obtainable in a matched Al system.

As has been detailed in the progress reports, we have modified our bonding equipment and now have significantly better control of our bonding process. It is controllable so that we can get excellent balanced interface welds, weld deeply into the substrate, or weld deeply into the bumps when we have consistant Al on both items. We have been able to consistantly weld 93L415 memory die to a 3.5 x 2.5 ceramic substrate with 16 bump 4 x 4 mil pads. Two 4096 x 9 bit memory planes are being furnished to AFML for additional evaluation of the all-aluminum bump die attachment; the bonds on these substrates are typical of our present capabilities. The bond shear strengths average over 1000 grams per die. During our development program we have increased our attachment proof test from 400 grams to 700 grams for these die. We are getting good results in repairability of these substrates. The same bonding equipment was used for the 6 bit adders. We have thus used our latest bonding equipment and techniques but unfortunately not on properly matched Al. This implies that better bonds than those on most parts delivered on this contract are feasible and reasonable on new designs using our now available knowledge about the processes.

A third area of knowledge has now been expanded since the 6-bit adder substrates were designed and fabricated. At the time they were designed, it was believed that the contact area on the substrate should be about the same as the bump surface. If everything were perfect this

is perhaps theoretically true. However, in the real world we find that masking tolerances on the pads and bumps and location tolerances during bonding tend to misalign pads and bumps. This will cause the parts to "move" or "rotate" during bonding. The bonding power and time (and sometimes pressure) are reduced to keep rotation or translation to a minimum. This results in a less than optimum bond strength. Unfortunately this knowledge came to the surface long after the 6-bit adder substrates were designed and processed. In future designs it will be just as easy to make the "pad area" great enough so that it exceeds the bump size by at least one mil on each side. This will allow use of optimum bonding parameters and will result in better bond strengths.

IN SUMMARY

- The 9702 and 9708 die do not have optimum Al bump characteristics.
- The mask designs on the substrate did not properly account for mechanical tolerances between lower and upper layer metal. (i.e., resulting in small pads).
- The substrate pad design is not large enough to reduce rotation and movement on bonding.
- The two masks used in processing die bumps did not give optimum flat bump surfaces and sizes.
- The new bonding tools and procedures were utilized.
- The latest die and substrate cleaning procedures were used.

It follows that: With a new design and using the latest techniques, considerably better bonds will result. The shear strength of the die will be much greater and the uniformity of welds on each bump within a die can be improved. It is respectfully suggested that in any failure analysis performed conclusions should be drawn from the die that had the "best" attachments rather than the "poorest". We expect that the "worst" bonds using the latest processing methods and designs will exceed the best obtained on this project.

REFERENCES

1. A. J. Learn and W. H. Shepherd, "Reduction of Electromigration - Induced Failure in Aluminum Metallization Through Anodization" Proceedings, Reliability Physics Symposium, P. 129, March 1971, Las Vegas.

   A. J. Learn, "Effect of Structure and Processing on Electromigration-Induced Failure in Anodized Aluminum" J. App. Physics, 44, 1251 (1973).

2. C. J. Dell'Oca and A. J. Learn, "Anodization of Aluminum to Inhibit Hillock Growth During High Temperature Processing", Thin Solid Films, 8 (1971) R47-R50.

3. C. J. Dell'Oca and P. J. Fleming, "Growth Properties of the Barrier Portion of Porous Anodic Alumina Films," presented at the Electrochemical Society Fall Meeting, 1971. Extended Abstract #84.

4. J. P. O'Sullivan and G. C. Wood "The Morphology and Mechanism of Formation of Porous Anodic Oxide Films on Aluminum", Proc. Royal Society of Lond, A. 317, 511 (1970).

5. C. J. Dell'Oca, "Properties of Anodic Oxide Films Formed in the Anodization of Silicon Nitride", Fairchild Internal Technical Report #543.

6. L. Young, "Anodic Oxide Films" Pergammon Press 1961.

7. D. Pilling "Anodic Oxidation of Silicon For MOS Capacitors and Integrated Circuits", Fairchild Internal Publication.

8. C. J. Dell'Oca and M. L. Barry "The Combination of Silicon Nitride and Aluminum Anodization for Semiconductor Device Passivation", Solid State Electronics 15, 659 (1972).

APPENDIX

TTL ISOPLANAR HYBRID MEMORY

4096 X 9 BIT FULLY DECODED RANDOM ACCESS PLANE

DESCRIPTION

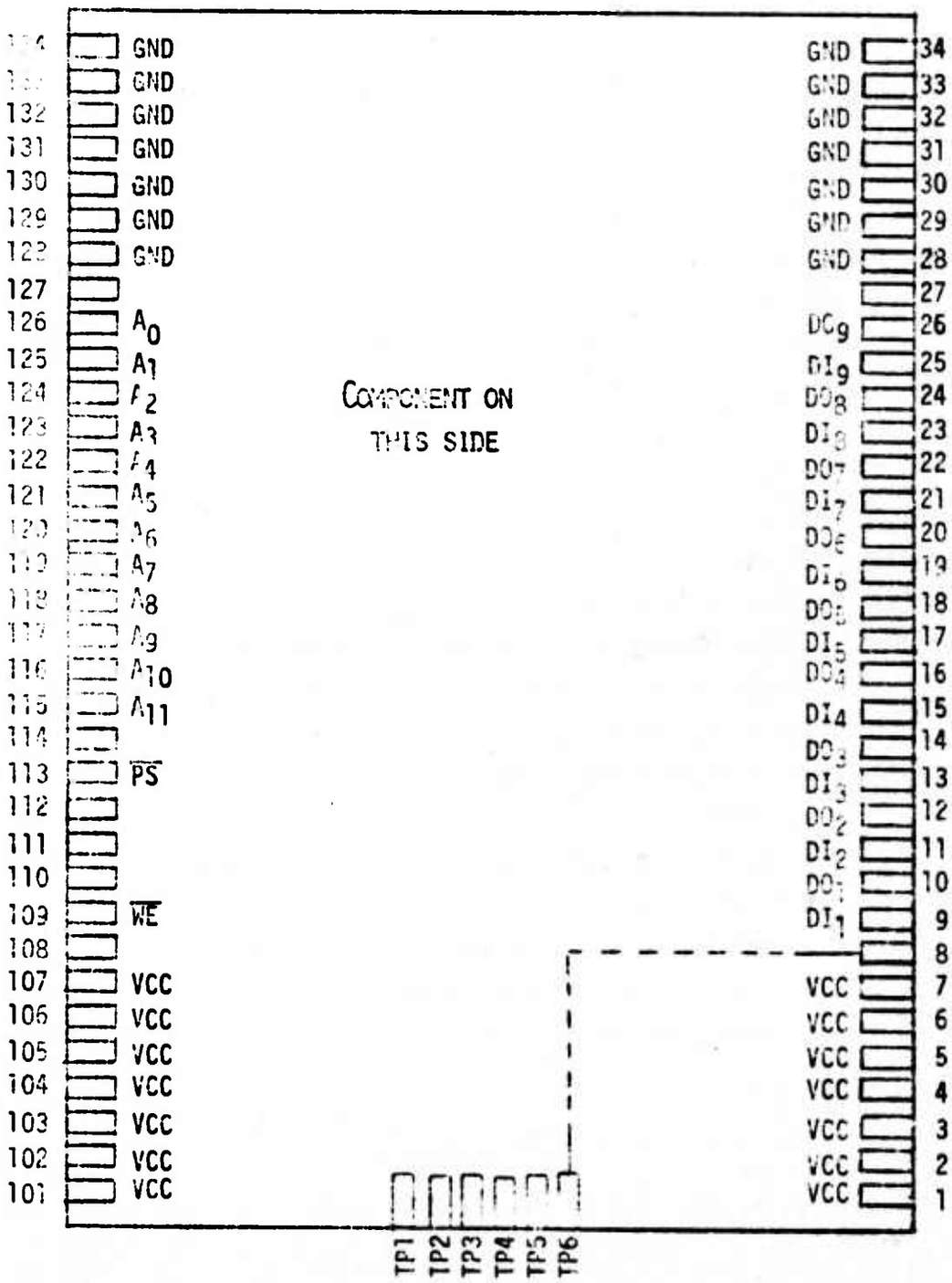
The 4K x 9MCM-1 plane is a 4096 x 9 bit read/write random access memory plane organized with 4096 words of 9 bits each. It has a typical read access time of 76 nsec and is designed for high performance memory applications. The plane is on a 2.5 inch by 3.5 ceramic base. Planes may be mounted on .70 inch centers.

The plane has separate data input and data output lines and a plane select line which is active when low. The plane is fully compatible with the standard DTL and TTL logic families. Each data out is a wired "or" connection of five 93415 T^2L RAM's. The wired "or" connection is left in the uncommitted collector output configuration.

- TTL Inputs and outputs
- Non-inverting data output
- Organized 4096 words x 9 bits
- Read access time 76 nsec typical
- Power dissipation max 31.4 watts (6.3 amps at 5.0 volts)
- Cooling required - forced air
- Small physical size 2-1/2" x 3-1/2" (X.70")
- Standard printed circuit board edge connector spacing is used (pins on 0.1" centers)

INPUT PIN NAMES		LOADING
$\overline{PS}$	Plane Select	1.25 U.L.
A_0, A_1, A_2, A_3, A_4, A_5, A_7	Address Inputs	3.75 U.L.
A_8	Address Inputs	6.25 U.L.
A_6, A_9, A_{10}, A_{11}	Address Inputs	5.00 U.L.
$\overline{WE}$	Write Enable	1.25 U.L.
DI_1 through DI_9	Data In	1.25 U.L.

CONNECTION DIAGRAM (4MX9 MCM-1)



Test points are only used during construction.

OUTPUT PIN NAMES		DRIVE CAPABILITY
DO_1 through DO_9	Data Out	10.00 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

FUNCTIONAL DESCRIPTION

The 4K x 9MCM-1 is a fully decoded 36,865 bit random access memory organized with 4096 words by 9 bits. Word selection is achieved by means of a 12 address bits numbered A_0 through A_{11}.

One plane select input is provided for memory array expansion. This plane select is active low.

The read and write operations are controlled by the state of the "active low" write enable pin 109. With $\overline{WE}$ held low and the plane selected (LOW) the data at the data input pins DI_1 through DI_9 is written into the addressed location. To read $\overline{WE}$ is held high and the plane is selected. Data in the specified location is presented at data outputs DO_1 through DO_9 and is non-inverted.

To minimize cost per bit the 4K X 9 MCM-1 utilizes 1024 bit memory die which do not have all the bits operation. A redundancy system is used where a fifth die substitutes good bits at specific addresses for each of four other die which have corresponding inoperative bits at these locations. Chip select decoding logic is included on the plane so the user is not concerned with this logic. The decoding time is less than normal data access time and therefore does not increase the memory acces or cycle times. This technique accounts for the input unit loads and output drive capabilities listed. The data out pin is a wired "or" configuration of five 93415 die with uncommitted collectors. In memory expansion each of the data outputs of one plane may be tied to the corresponding data out pins of another plane or planes. In applications which require maximum speed, the wired "or" configuration of planes would

not be used. In either case, an external pull-up resistor of value RL must be used to provide a logic one (1) at the output when it is off. Any value of RL within the range specified below may be used.

$$\frac{V_{CC}\ (MAX)}{I_{OL}\ -F.O.\ (1.6\ mA)} \leq RL \leq \frac{V_{CC}(MIN)\ -V_{OH}}{N(I_{CEX})\ +\ F.O.\ (0.04\ mA)}$$

RL is in KΩ

N.....Number of 93415 wired OR outputs tied together (each plane has five 93415 outputs internally wired together).

F.O. .....Number of TTL unit loads driven

I_{CEX}.....4K X 9 MCM-1 memory plane output leakage current (250 μA Max.).

V_{OH} .....Required output HIGH level at output mode.

I_{OL} .....Output LOW current for 93415 die (16 mA).

The minimum value of RL is limited by output current sinking ability. The minimum value of RL also provides the fastest rise time for the data out. The maximum value of RL is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}.

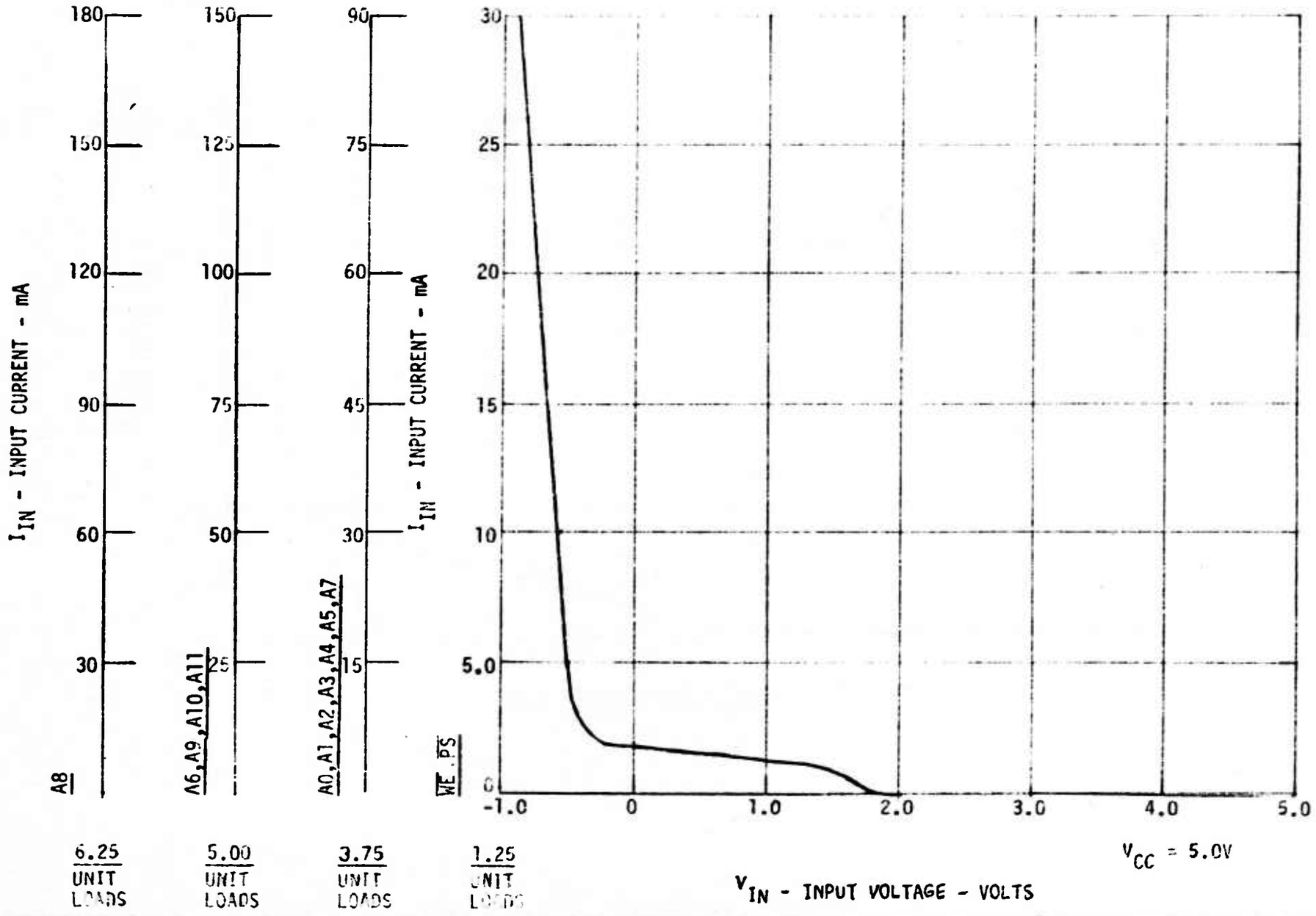
TYPICAL INPUT AND OUTPUT CHARACTERISTICS

TABLE 1 - TRUTH TABLE

INPUTS				MODE
$\overline{PS}$	$\overline{WE}$	I_{1-9}	DO_{1-9} OPEN COLLECTOR	
H	X	X	H	NOT SELECTED
L	L	L	H	WRITE "0"
L	L	H	H	WRITE "1"
L	H	X	L=0; H=1	READ

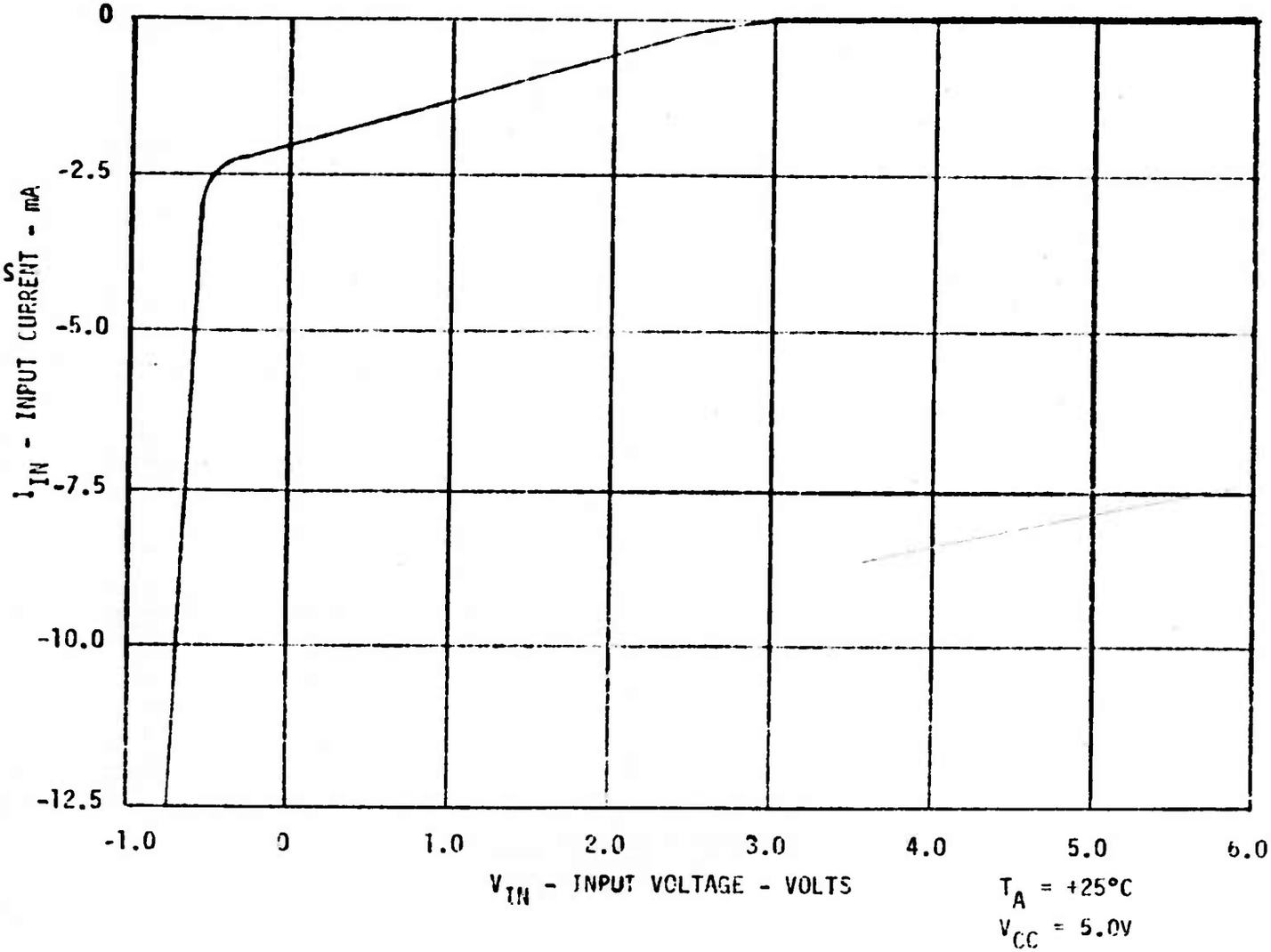
H = High Voltage; L = Low Voltage; X = Don't care high or low.

TYPICAL INPUT CHARACTERISTICS
SCHOTTKY INPUT (1.25UL)



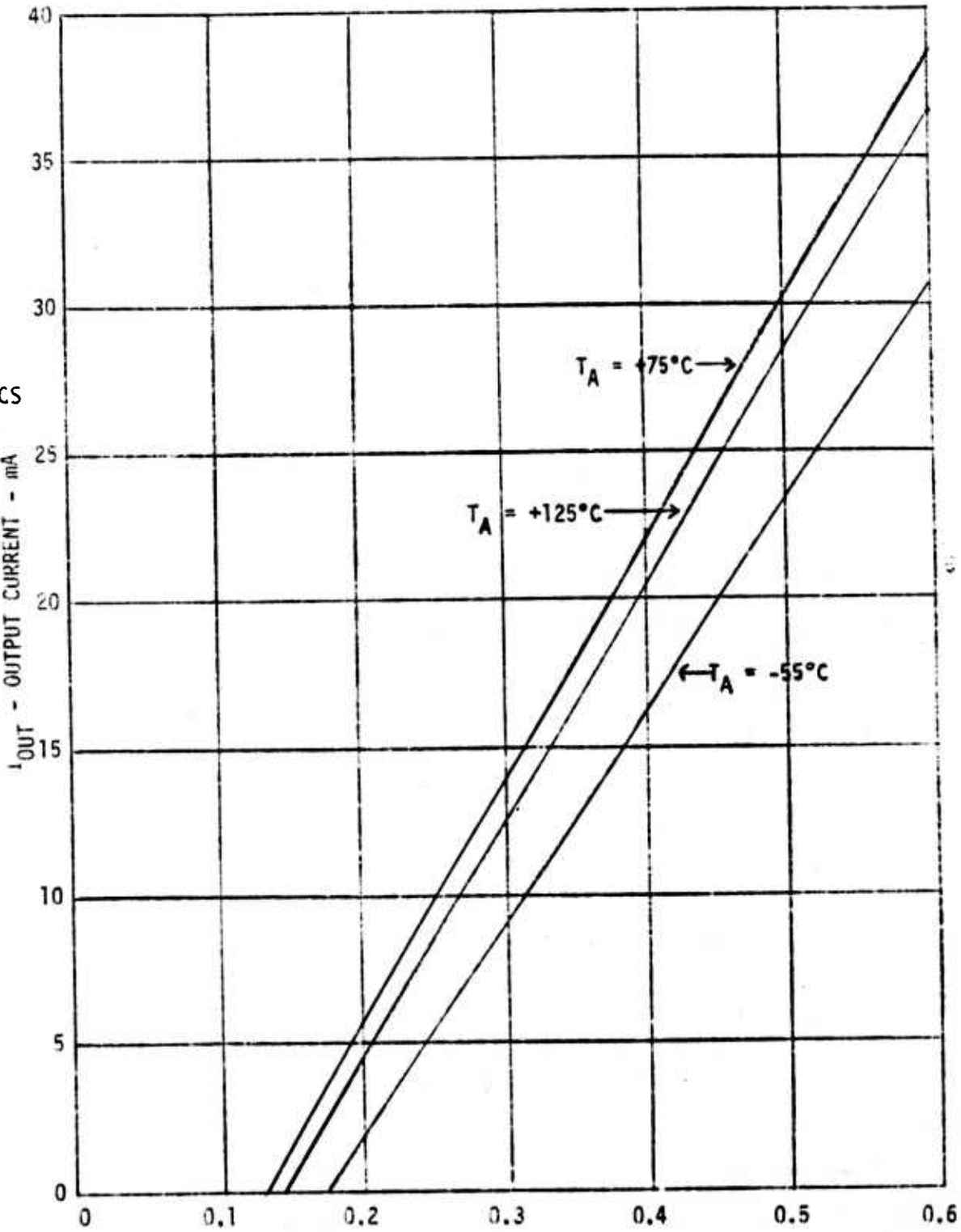
INPUT CHARACTERISTICS FOR DI_1 - DI_9

INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (LOW STATE)

OUTPUT CHARACTERISTICS FOR DO_1 - DO_9



T_A = +25°C
V_{CC} = 5.0V

ABSOLUTE MAXIMUM OVERLOAD RATINGS (above which useful life may be impaired)

Storage Temperature	-65°C to +100°C
Temperature under bias (with cooling air)	+20°C to +55°C
V_{CC} pin potential to ground pin	-0.5 V to +5.5 Volts
Voltage applied to outputs (output HIGH)	-0.5 V to +5.5 Volts
Output current (DC) (Output LOW)	+20 mA
Input Voltage (DC)	-0.5 V to +5.5 Volts

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT AIR INLET TEMPERATURE
	MIN	TYP	MAX	
4K X 9 MCM-1	4.75	5.0	5.25	+20°C to +55°C

DC CHARACTERISTICS

SYMBOL	CHARACTERISTICS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
V_{OL}	Output LOW Voltage	--	0.3	0.45	V	V_{CC} = Min., I_{OL} = 16mA
V_{IH}	Input HIGH Voltage	2.1	--	--	V	Guaranteed input HIGH Voltage for all inputs
V_{IL}	Input LOW Voltage	--	--	0.8	V	Guaranteed input LOW Voltage for all inputs
I_{CEX}	Output Leakage Current	--	5.0	250	uA	V_{CC} = Max., V_{OUT} = 4.5 Volts
V_{CD}	Input Diode Clamp Voltage	--	-0.65	-1.2	V	V_{CC} = Min., I_{IN} = -18mA
I_{CC}	Power Supply Current		?	6.34	amps	V_{CC} = Max., $T_A \geq 25°C$
I_{IL}	Input LOW Current					
	$\overline{PS}$	--	-1.4	-2.0	mA	V_{CC} = Max., V_{IN} = 0.5V
	$A_0 - A_7$	--	-4.2	-6.0	mA	V_{CC} = Max., V_{IN} = 0.5V
	A_8	--	-7.5	-10.0	mA	V_{CC} = Max., V_{IN} = 0.5V
	$A_9 - A_{11}$	--	-5.6	-8.0	mA	V_{CC} = Max., V_{IN} = 0.5V
	$\overline{WE}$	--	-1.4	-2.0	mA	V_{CC} = Max., V_{IN} = 0.5V
	$I_1 - I_9$	--	-1.25	-2.0	mA	V_{CC} = Max., V_{IN} = 0.4V
I_{IH}	Input HIGH Current					
	$\overline{PS}$	--	1.0	50	uA	V_{CC} = Max., V_{IN} = 2.7V
		--	--	1.0	mA	V_{CC} = Max., V_{IN} = 5.5V
	$A_0 - A_7$	--	3.0	150	uA	V_{CC} = Max., V_{IN} = 2.7V
		--	--	3.0	mA	V_{CC} = Max., V_{IN} = 5.5V
	A_8	--	5.0	250	uA	V_{CC} = Max., V_{IN} = 2.7V
		--	--	5.0	mA	V_{CC} = Max., V_{IN} = 5.5V
	$A_9 - A_{11}$	--	4.0	200	uA	V_{CC} = Max., V_{IN} = 2.7V
		--	--	4.0	mA	V_{CC} = Max., V_{IN} = 5.5V
	$\overline{WE}$	--	1.0	50	uA	V_{CC} = Max., V_{IN} = 2.7V
		--	--	1.0	mA	V_{CC} = Max., V_{IN} = 5.5V
	$I_1 - I_9$	--	5.0	200	uA	V_{CC} = Max., V_{IN} = 4.5V
		--	--	5.0	mA	V_{CC} = Max., V_{IN} = 5.25V

AC CHARACTERISTICS

SYMBOL	ITEM	CHARACTERISTIC MIN	CHARACTERISTIC TYP	CHARACTERISTIC MAX.	UNITS	CONDITIONS
	READ MODE					
T_{AR}	Address Stable Time	76	--	--	ns	V_{CC} = +5.0 and T_A = +25°C
T_{SR}	Plane Select Stable Time	76	--	--	ns	V_{CC} = +5.0 and T_A = +25°C
T_R	Read Select HIGH	76	--	--	--	Should remain HIGH when not writing
T_{DO}	Data Access Time	76	76	80	ns	TYP: V_{CC} = +5.0V and T_A = +25°C
T_{DH}	Data Hold Time	10	10	10	ns	Lengthen T_{AR} and T_{SR} to lengthen T_{DH}
	WRITE MODE					
T_{AW}	Address Stable Time	103	103	110	ns	V_{CC} = +5.0 and T_A = +25°C
T_{SW}	Plane Select Stable Time	103	103	110	ns	V_{CC} = +5.0 and T_A = +25°C
T_{WSA}	Address Set-up Time	27	--	--	ns	V_{CC} = +5.0 and T_A = +25°C
T_W	Write Pulse Width	61	--	--	ns	V_{CC} = +5.0 and T_A = +25°C
T_{WHA}	Address Hold Time	15	--	--	ns	V_{CC} = +5.0 and T_A = +25°C
T_{WD}	Data Don't Care Time	--	--	25	ns	V_{CC} = +5.0 and T_A = +25°C
T_{WSD}	Data Set-up Before Write	2	--	--	ns	V_{CC} = +5.0 and T_A = +25°C
T_{DI}	Data Stable Time	78	78	95	ns	V_{CC} = +5.0 and T_A = +25°C

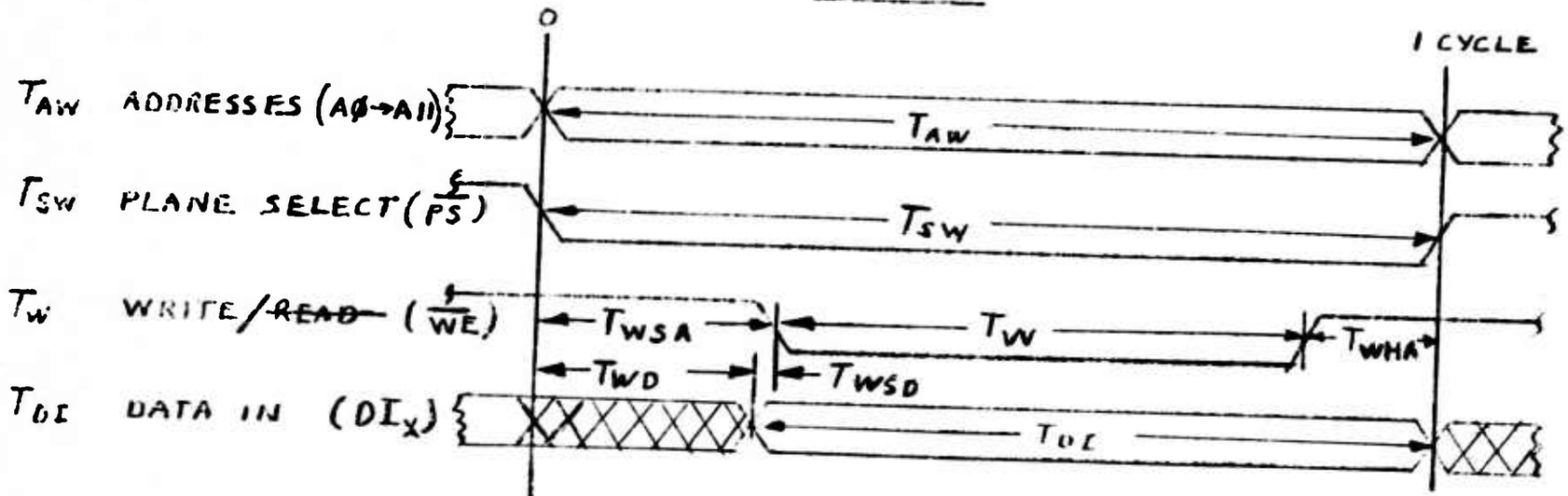
V_{CC} = +5.0V + .25V
$T_{Ambient}$ = +20°C - +55°C

NOTES:

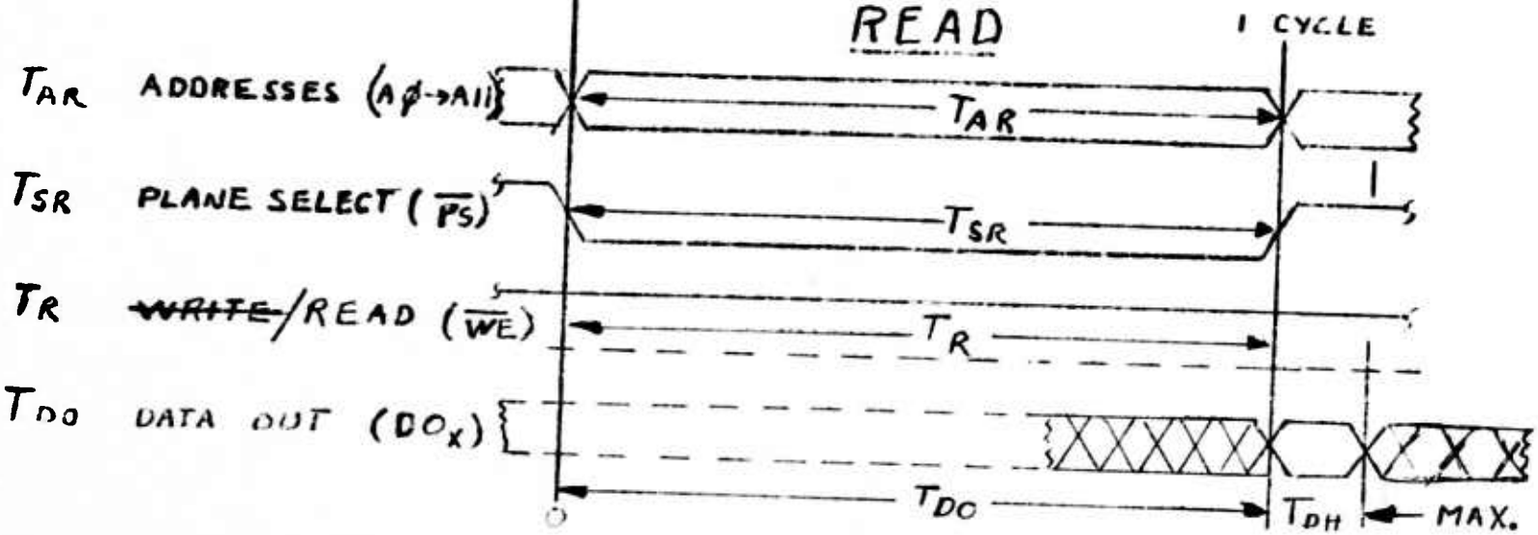
1. Plane should warm up two minutes before use.
2. Forced air flow of 400 feet per minute is assumed.
3. MIN and TYP values are for V_{CC} = +5.0 V and T_A = +25°C.
4. MAX values are for worst case voltage, Loading and Temperature.
5. The T_{AR}, T_{SR}, and T_R waveforms may be lengthened any amount desired to provide longer cycles and longer "Data Output" Stable Times (i.e., T_{DH}).
6. The T_{WSA}, T_W, T_{WHA}, T_{WSD}, and T_{DI} minimum times will guarantee that the proper location will be WRITTEN into and that no other location will be changed. This applies to any mixture of WRITE and READ cycles. Longer T_{AW} and T_{SW} times may be used if desired. If the T_{WHA} minimum condition is met T_W and T_{DI} may also be lengthened as desired.
7. T_{DO} should be strobed during T_{DH} time to insure that proper data is on the Data Output lines.

SWITCHING WAVE FORMS: 4K x 9 MCM-1

WRITE



READ



PACKAGE INFORMATION

68 Lead 4K X 9 MCM-1